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Electrochemical Sensor System Architecture Using The CMOS-MEMS Technology For Cytometry Applications

Marek Sebastian Piechocinski

A THESIS SUBMITTED TO
SCHOOL OF ENGINEERING
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"The present is theirs; the future, for which I really worked, is mine"

Nikola Tesla

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Abstract

This thesis presents the development process of an integrated sensor-system-on-chip for recording the parameters of blood cells. The CMOS based device consists of the two flow-through sensor arrays, stacked one on top of the other. The sensors are able to detect the biological cell in terms of its physical size and the surface charge on a cell's membrane. The development of the measurement system was divided into several stages these were to design and implement the two sensor arrays complemented with readout circuitry onto a single CMOS chip to create an on-chip membrane with embedded flow-through micro-channels by a CMOS compatible post-processing techniques to encapsulate and hermetically package the device for liquid chemistry experiments, to test and characterise the two sensor arrays together with readout electronics, to develop control and data acquisition software and to detect the biological cells using the complete measurement system. Cytometry and haematology fields are closely related to the presented work, hence it is envisaged that the developed technology enables further integration and miniaturisation of the biomedical instrumentation.

The two vertically stacked 4 x 4 flow-through sensor arrays, embedded into an on-chip membrane, were implemented in a single silicon chip device together with a readout circuitry for each of the sensor sets. To develop a CMOS-MEMS device the design and fabrication was carried out using a commercial process design kit (0.35 μm 4-Metal, 2-Poly, CMOS) as well as the foundry service. Thereafter the device was post-processed in-house to develop the on-chip membrane and open the sensing micro-apertures. The two types of sensor were integrated on the silicon dice for multi-parametric characterisation of the analyte. To read the cell membrane charge the ion sensitive field effect transistor (ISFET) was utilised and for cell size (volume) detection an impedance sensor (Coulter counter) was used. Both sensors rely on a flow-through mode of operation, hence the constant flow of the analyte sample could be maintained. The Coulter counter metal electrode was exposed to the solution, while the ISFET floating gate electrode maintained contact with the analyte through a charge sensitive membrane constructed of a dielectric material (silicon dioxide) lining the inside of the micro-pore. The outside size of each of the electrodes was 100 μm x 100 μm and the inside varied from 20 μm x 20 μm to 58 μm x 58 μm. The sense aperture size also varied from 10 μm x 10 μm to 16 μm x 16 μm. The two stacked micro-electrode arrays were layed out on an area of 500^2 μm^2.

The CMOS-MEMS device was fit into a custom printed circuit board (PCB) chip carrier, thereafter insulated and hermetically packaged. Microfluidic ports were attached to

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the packaged module so that the analyte can be introduced and drained by a flow-through mode of operation. The complete microfluidic system and packaging was assembled and thereafter evaluated for correct operation. Undisturbed flow of the analyte solution is essential for the sensor operation. This is related to the fact that the electrochemical response of both sensors depends on the analyte flow through the sense micro-apertures thus any aggregation of the sample within the microfluidic system would cause clogging of the micro-pores.

The on-chip electronic circuitry was characterised, and after comparison with the simulated results found to be within an error margin of what enables it for reliable sensor signal readout.

The measurement system is automated by software control so that the bias parameters can be set precisely, it also helped while error debugging. Analogue signals from the two sensor arrays were acquired, later processed and stored by a data acquisition system. Both control and data capture systems are implemented in a high level programming language. Furthermore both are integrated and operated in a one window based graphical user interface (GUI).

A fully functional measurement system was used as a flow-through cytometer for living cells detection. The measurements results showed that the system is capable of single cell detection and on-the-fly data display.

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1. B. Nemeth, M.S. Piechocinski, D. R. S. Cumming, "High-resolution real-time ion-camera system using a CMOS-based chemical sensor array for proton imaging", *Sensors and Actuators B: Chemical*, 171-172. pp. 747–752, August-September 2012.

2. M. S. Piechocinski, J. Grant, P. Shields, D. R. S. Cumming, "Coulter-counter and ISFET dual sensor micro-aperture flow-through CMOS array", *IEEE Transactions on Biomedical Circuits and Systems*, 2012. (submitted).

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1. M. S. Piechocinski, D. R. S. Cumming, "Integration of Coulter Counter and pH Sensor on a Single Chip Using Standard CMOS 0.35 μm Technology", *University of Glasgow, Postgraduate Research Conference,* Glasgow, United Kingdom, Feb. 2008.

2. D. R. S. Cumming, P. N. Shields, M.S. Piechocinski, B. Nemeth, "High speed sensing using ion sensitive field effect transistors", *IEEE International Worksop on Advanced on Sensors and Interfaces (IWASI)*, pp. 57 – 59, Savelletri di Fasano, Italy, June 2011

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1. Ata Khalid, Shimul C. Saha, Yong Ma, James P. Grant, Marek S. Piechocinski and David R. S. Cumming, "THz Systems and Technology", *I-nano Day*, Glasgow, United Kingdom, Oct. 2010.

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3. P. G. A. MacPherson, A. L. Bernassau, M. S. Piechocinski, M. Rhiele, D. R. S. Cumming, "Integration of acoustic tweezers and a microfluidic sensor system", *Sonotweezers, Project Meeting*, Glasgow, United Kingdom, 2012.

Contribution to other projects:

Post-processing and SEM imaging:

1. A. Ibrahim, D. R. S. Cumming, "Passive single chip wireless microwave pressure sensor", *Sensors and Actuators A: Physical*, 165 (2). pp. 200 – 206, Nov. 2010.

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Beinn a’ Chroin were my favourite, however some peaks in the High Tatra Mountains are still unmatched.

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1 Introduction to the Research

1.1 Introduction

This section of the thesis describes the motivation for the presented biomedical research reflecting both application and technology. Furthermore the research capability and key objectives of the work are identified. Thereafter, a structure of the thesis is outlined.

1.2 Motivation and Technology

The study of cellular behaviour and their number in population has been used for decades to understand and assess the properties of blood, and thereby the operation of the vital organs and immune system in the body [1]. Initially the cell number in the analyte sample and its basic properties, i.e. size and shape, were assessed under an optical microscope by trained laboratory technicians. The processing time and quality of the sample assessment were limited by the skills and experience of the operating personnel. The sample interrogation by manually positioning it under an optical microscope gives a planar view of the specimen, it does not output any information about the ionic concentration on the cell membrane as well as suspension medium chemistry. A biological cell suspended in a buffer solution exchanges ions and other products through its membrane. Ion exchange takes place through the entire life cycle of the cell thus indicates cell activity and metabolism [2]. The distribution of the ionic species on the cell plasma membrane is specific to the function and properties of the cell. What is more, the ionic concentration on the membrane is related to the cell health state, therefore the technology capable of measuring the membrane charge parameter [3] is highly desirable. Another electrical parameter of the biological cell, its impedance, is a carrier of unique information related to the size, membrane thickness and the interior properties of the cell [1]. Therefore, an automated and multi-parametric analysis of the cellular population on a single cell basis is an essential requirement for multiple fields of security [4], biomedical and biotechnological [5] applications. To enable automated interrogation of the characteristics of the cellular species the flow cytometry technique was developed in the early 1950's [6, Chapter1]. Increasing needs for methods and devices that could measure various parameters of a cell led to development of highly sophisticated multi-parametric flow cytometers capable of recording over ten features for each analyte sample. However these multi-parametric systems due to their complexity are large in size and cost effective usually while in constant operation in centralised bio-medical laboratory environments where it can achieve a high sample throughput. The impedance based flow cytometry technique [7] is of particular interest

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since its scalability and capability of being highly miniaturised enables for easy integration with a readout circuitry using the CMOS[1] technology.

To date, the majority of miniaturised impedance based flow cytometer devices use lateral flow techniques [7]. However, the lateral method encounters significant limitations when scaling down the device. The number of lateral sensing apertures that can be developed on a single micro-chip is limited due to the space required for an electrode layout as well as a discrete microfluidic channel that is required on top of each of the sense electrode sets. Therefore, parallelisation of the measurement method by using an array-like sense aperture layout is difficult to achieve, especially on a small (sub-millimetres) area. The vertical electrode layout [8] overcomes these limitations by integrating these microfluidic channels into the device. The vertical device allows for there to be many apertures laid out in an array so that the overall fluid flow rate, hence the cell parameters recording speed, may be increased. Parallelisation in this manner is achieved by embedding electrodes into the side-walls of each micro-aperture in the array so that independent counts can be made. Furthermore the overall device dimensions can be scaled down without diminishing the throughput of the device. The flow-through sensing methodology combined with a multi-metal layer CMOS device gives an opportunity to implement multiple sensing electrodes in each of the micro-apertures. What is more it enables various sensors to be implemented in one pore. One such sensor is the flow-through ISFET[2] [9]. This sensor is capable of measuring the ionic concentration in the analyte solution.

In this work, a sensor system combining the two flow-through arrays integrated onto a single CMOS chip, together with the interface electronics, is developed to measure single cell properties. The commercial CMOS technology used to develop the device is widely propagated across the microelectronic industry and is the backbone for state-of-the-art electronic equipment due to its reliability. What is more scalability, batch manufacturing and low cost production enable CMOS technology to be a suitable platform for complex sensor systems integrated with sophisticated application specific electronic circuitry [10]. As a consequence the SSoC[3] is able to perform a multi-parametric measurement and output a meaningful set of data for a specific biological analyte sample.

The developed technology presents benefits for chemical and biomedical applications including new drug research and testing, therapy monitoring and as portable hand-held equipment for liquid analyte interrogation. For instance, by utilising the proposed measurement system for studying the cells in suspension, it would be possible to character-

[1] Complementary Metal Oxide Semiconductor.
[2] Ion Sensitive Field Effect Transistor.
[3] Sensor System on Chip.

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ise the influence of a new drug on a basic building block (cell) in a living organism. Another emerging discipline where the technology can be used is the low cost portable cytometry instrument, performing multi-parametric analysis on a blood sample and outputting meaningful data which can enable medical personnel to counteract quicker or to have deeper insight into the disease pathology.

The developed technology presents a novel approach for increasing the throughput of the system by utilising an array of micro-fluidic channels. Analyte flows through all apertures simultaneously enabling a high speed parallel measurement. What is more the developed platform enables a multi-parametric readout from the aperture due to the two different sensors integrated in each of the pores. This particular feature is unique and shows a possibility of integration of multiple sensors within a single micro-channel. Another novelty of this work is the scalability of the device in various directions. Some of which are; the number of apertures can be increase which will magnify the throughput, decreasing the aperture size will enable sensing of small molecules, and finally increasing the number of sensors per aperture will allow acquiring even more informations about the analyte sample. Furthermore the SSoC is developed in a standard CMOS technology creating a potential for cost efficient and high volume production.

1.3 Research Aim and Objectives

The presented work focusses on techniques and methods that enabled development of an integrated sensor-system-on-chip utilising a standard CMOS technology. The aim of this research is to develop a CMOS-MEMS[4] device for a flow-through biological cell analysis.

The primary objective is to turn the concept into a design for an integrated sensor system on chip using commercial CMOS technology. Furthermore the on-chip electronic circuitry has to be sturdy enough to withstand the post-process in high density plasma. The sensors in both stacked arrays have to be independently addressable thus the switching and digital addressing circuitry will be engineered. Both sensors are directly capable of measuring analyte properties. An electrode layout will be designed in the form of a rectangular frame so that in its centre the sense micro-aperture can by created by front and back-side postprocessing means. The layout complying with the CMOS design rules will be taped out to a foundry for manufacturing.

The second objective is to develop the CMOS compatible post-processing methods at a chip level for the front and back-side of a silicon dice so that the on-chip membrane with micro-pores can be engineered. Focussed ion beam (FIB) milling is a desirable

[4] Micro Electro Mechanical Systems.

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method for the front-side oxide layers post-processing and a deep reactive ion etching (DRIE) is suitable for the back-side silicon substrate removal. Wet etch techniques are avoided due to their highly isotropic profile.

The third objective is to establish and implement an encapsulation and packaging method for the flow-through mode of operation of the sensor system. Unpackaged silicon dices are required to be returned from the foundry, this is related to the fact that each chip has to be post-processed, furthermore encapsulated and packaged. Water proof and hermetic casing are the key requirements for the wafer-level chip-scale package (WL-CSP). This will allow use of the sensor module for electrochemical and biological experiments. Working with the electrochemical sensors for wet chemistry sensing applications is not trivial, therefore this task will require a multidisciplinary approach to develop the microfluidic housing for the flow-through system.

The fourth objective is to test and characterise the electronic counterparts of the sensor system. It will be necessary to establish reliable and repeatable experimental procedure that allows output of meaningful data from the two types of sensors. Measurements with various analyte solutions will be taken to observe and characterise the response of the system. This will allow assessment of the performance of the technology.

The fifth and final objective is to run the experiments fully automated and integrated with a data acquisition and control software. Measurement system control and data acquisition software written in a high level programming language will control the hardware instrumentation over the general purpose interface bus (GPIB) and acquire data over the universal serial bus (USB). Thereafter the system will be used for living cells detection to demonstrate the technology capability.

1.4 Thesis Outline

The remainder of this thesis is divided into seven chapters.

Chapter 2 is a review of the scientific literature relevant to the development of an integrated sensor system on a CMOS chip for microparticle and biological cell detection.

Chapter 3 introduces the model of a microparticle in a suspension solution as well as the theory of operation of the Coulter counter and ISFET based ion sensor.

Chapter 4 outlines the design process of an active sensor system, circuitry and its implementation in CMOS technology.

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Chapter 5 discusses the CMOS compatible post-processing techniques utilised to develop an on-chip membrane with micro-apertures.

Chapter 6 provides details of the sensor system and readout electronics characterisation. Techniques and procedures for experimental setup are discussed.

Chapter 7 describes the measurement system control and data acquisition process in order to perform cytometry operation with a single cell resolution.

Chapter 8 draws conclusions from the presented work and gives suggestions for future work in the field of sensor system on chip.

There are also four appendices providing additional data. These have been separated from the main body for the sake of clarity. Appendices include electrical circuit diagrams as well as the main modules of the control and data acquisition software. Note that copy of the software source code is contained on a DVD-ROM to make it more accessible to the reader.

1.5 Summary

The motivation for this work has been introduced by describing the research field in which the project was embedded. Furthermore, the potential applications for the technology were given and short examples were highlighted. The research aim and objectives were identified and an outline for the thesis was given. In the following section the scientific literature relevant to the presented work will be reviewed.

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2 Literature Review

2.1 Introduction

This chapter contains a review of the literature relevant to the development of a sensor system on a chip. The system consists of an array of two types of sensors: a Coulter counter for cell counting and a pH meter. The background and history of both cell and microparticle counting is described, followed by system integration on chip. The chapter then moves on to discuss the microfabrication and CMOS compatible post-processing techniques that have been developed and adapted to CMOS devices. Finally the adapted method for pH measurement is discussed.

2.2 Microparticle Characterisation Methods

Fluidic systems used for cell characterisation require technical solutions to be able to: identify, count, measure, sort, and separate single cells [11]. A principle of operation of the most commonly used platforms for microparticle and cell characterisation are based on three phenomena: light blocking and light scattering [12], electrical sensing zone [7] and inductive sensing [13], [14], [15], [16]. These systems deal with a large number of sample quantities therefore combining precise measurement with higher throughput [17], [18] will increase the amount of sample being analysed and detection of rare cells will increase. The flow cytometry[5] [6, Chapter 1] technique was developed to meet these requirements. Technology has developed from single parameter measurement to the latest highly integrated cytometry which is able to measure over 10 parameters of a single particle at the same time. Its operating principle (Skatron Argus 100 flow cytometer) is shown in Figure 2.1. This flow cytometry utilises fluorescence [19, Chapter 1] and light scattering [20, Chapter 1] methods for cell measurement and counting. The sheath of fluid is pumped through a narrow tube into which the sample is later injected. The sample is positioned in the middle of the fluid sheath by hydrodynamic focusing. The light scattering method uses light reflected from the microparticle [12]. As the sample flows through a measurement point (nozzle and cover slip) from the illumination source (mercury arc lamp) is scattered. The forward and right-angle light scattering events are measured by photomultipliers via optical filters and stored (processed) by software on to an attached computer. After measurement the sample flows into the waste tank. The advantage of flow cytometry with optical detection method is the high speed of counts: thousands of cells per second. More ad-

[5] General name for a number of methods used to measure various parameters of biological cells.

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vanced flow cytometry can also sort cells according to their size and their chemical properties [6, Chapter 1].

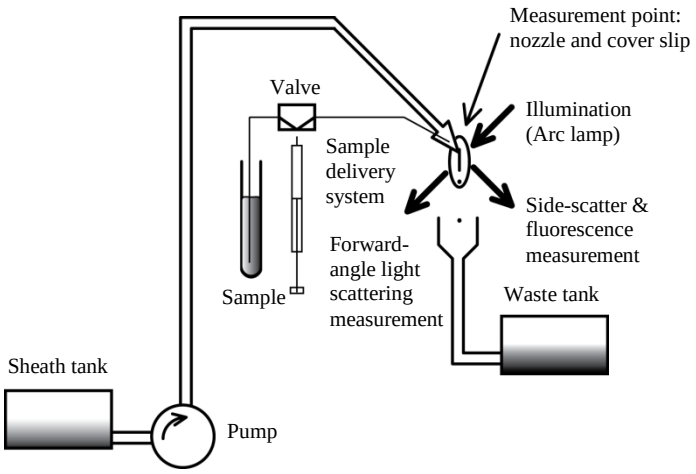

Figure 2.1: Flow cytometry operating principle [21].

Their main disadvantage is weight and cost. In the 1990s lab-on-a-chip (LOAC) technology evolved to the point that became interesting for both the commercial and research environment. Support came from military i.e. DARPA[6], their main interest was in portable biological and chemical weapon detection systems. Lab-on-a-chip [22, Chapter 1], [23] technology, also called Micro Total Analysis Systems (μTAS), offers a number of advantages eg. sensor integration, micro fluid handling (pumps, valves [24], mixing [25], cell sorting [26], separation [27]) and processing unit integration. Technology allows a non invasive and label free single cell differentiation against the size and its electrical properties. Both DC and AC methods are used for microparticle characterisation. The DC method is based on the resistance of the analyte. In the AC method there are two major ways of measuring the dielectrical properties of the cells: AC electrokinetics techniques and impedance spectroscopy. Using AC electrokinetics techniques like: dielectrophoresis [28], [29], [30], travelling wave dielectrophoresis [31], [32] and electrorotation [33], [34] particles' movement in microfluidic system can be studied. Utilising the AC electrical impedance spectroscopy [35] the electrical properties of the single particle or a cell suspended in a buffer solution can be measured [36, Chapter 7]. The AC method is particularly interesting as it allows for multi-parameter characterisation of a single particle. This will be discussed later in this chapter.

[6] Defense Advanced Research Projects Agency.

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2.3 Coulter Counter

The first instrument able to count particles and measure their size by employing an electrical measurement method was developed by Wallace Coulter [37]. The Coulter method is based on a DC electrical resistance measurement across a narrow aperture (Figure 2.2) connecting two fluid (conductive) filled containers. While the cell (dielectric sphere) passes through the aperture the resistance, which is measured by the upstream and downstream electrodes placed on both sides of the aperture, increases. The voltage pulse height that is produced corresponds to the cell's volume, and the pulse width is proportional to the particle's flow speed through the aperture.

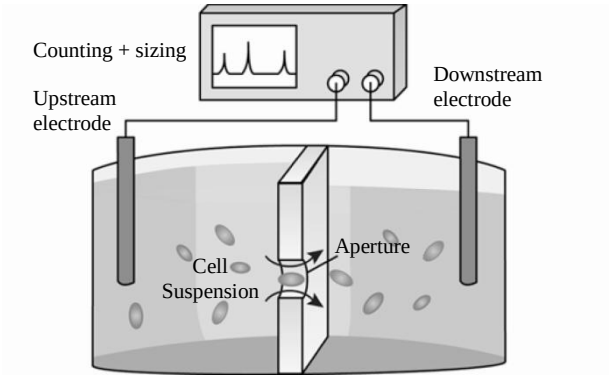

Figure 2.2: Coulter counter working principle while sensing cells [36, Chapter 7].

Each voltage pulse corresponds to one particle passing through the orifice. A simplified sketch of the aperture with microparticle [7] flowing through it is shown in Figure 2.3.

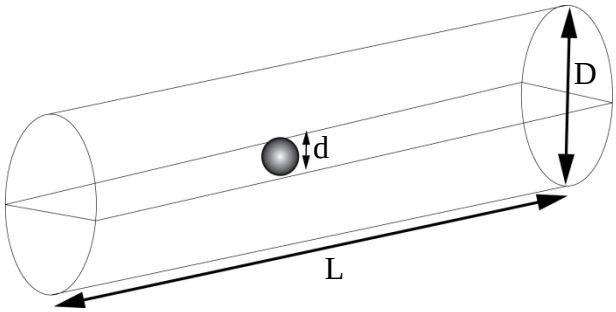

Figure 2.3: Aperture with microparticle.

The resistance of an aperture with liquid with diameter *D*, length *L* and electrolyte resistivity ρ_m is given by [38]:

$$R = \frac{4\rho_m L}{\pi D^2} \tag{2.1}$$

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Thus resistance change ΔR due to a particle with diameter *d* passing through an aperture is given by [38]:

$$\Delta R = \frac{4\rho_m d^3}{\pi D^2} \tag{2.2}$$

Wallace Coulter's device was able to count several thousand cells per second and provide the cell size distribution. The first Coulter counter was a single fluidic channel measurement device with sub-millimetre (~0.1 mm) aperture. Using direct current measurement method was a limiting factor for the first Coulter counter. The device was able to provide cells' sizes and distribution but there was no other information e.g. membrane capacitance and cytoplasmic conductivity.

2.3.1 Microfabricated Coulter counter

The first two developments of the microfabricated Coulter counter were published in 1990s. The first by Larsen [39] was a planar silicon structure with gold electrodes deposited on a glass lid, and the second by Koch [40] was a planar structure etched in silicon with titanium electrodes deposited inside a trench (Figure 2.4). The top of the microchannel was closed by a Pyrex wafer. Both publications did not present experimental results with cells or other microparticles.

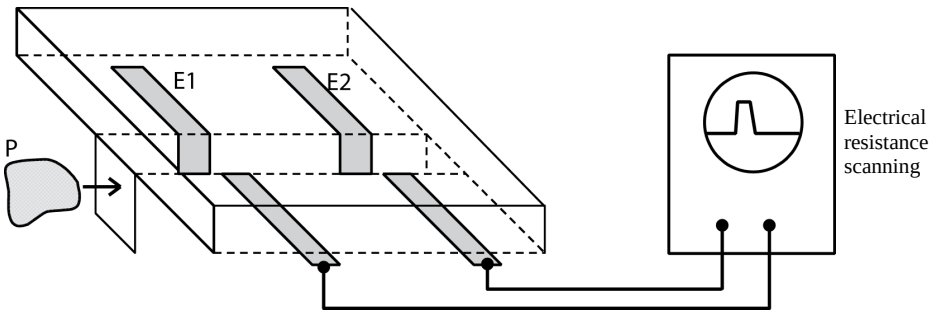

Figure 2.4: Micromachined Coulter counter, where: P – microparticle, E1 and E2 metal electrodes.

In 2001 a microchip Coulter counter was developed by Saleh and Sohn [41]. They fabricated the lateral device with pore dimensions: 5.1 µm x 1.5 µm x 1 µm shown in Figure 2.5. The device was fabricated on a quartz substrate by reactive ion etch process; metal (Ti/Pt) electrodes were deposited by metal evaporation and lift-off microfabrication process. The top of the reservoir was sealed by a silicon coated glass coverslip. The experimental result showed that the fabricated device was able to detect particles 460 nm in diameter by utilizing the DC resistance sensing technique (resistive pulse sensing [42]).

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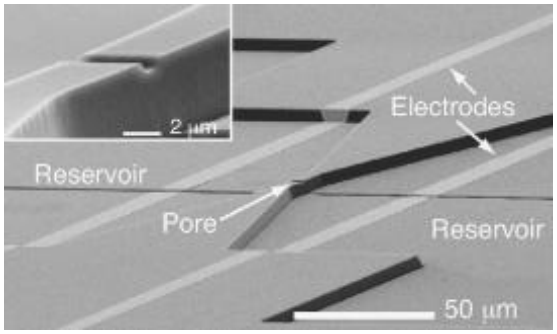

Figure 2.5: Scanning electron micrograph of the microchip Coulter counter.

Further development of the device, using soft lithography [43, Chapter 1] allowed fabrication of a sensing pore (1 μm wide) in polydimethylsiloxane (PDMS) on a glass substrate with deposited metal (platinum) electrodes (Figure 2.6 (a)) [44]. Decreasing its sensing aperture width to 200 nm revealed its potential in single DNA molecule sensing in early 2003 [45]. The pore is situated in the membrane between two containers filled with electrolyte solutions. While applying a potential difference to the electrodes on both sides of the membrane the ion current flowing through the pore with electrolyte solution can be measured. When DNA enters the pore it displaces electrolyte solution and the ion current is blocked, this results in a decreased measured current. The amplitude of the downward current pulse corresponds to displaced electrolyte solution inside the pore [46]. Experimental results from a DNA strand detection experiment can be seen in Figure 2.6 (b). The DNA strand detection has been done by using the concept of a microchip with a silicon nitride nano-pore. Two pore designs are shown the first with a 3 nm diameter and second with a 10nm diameter are located in a membrane 5 – 10 nm thick [47], [48]. The resistive pulse sensor technique has evolved to a stage that can be used for DNA detection [49], precise characterisation and sequencing [50] or antibody study [51]. The antibody study is particularly important in new drug studies and development processes. DNA sequencing requires particularly high throughput of the microfluidic measurement system as it deals with large sample amount. Integrating DNA sensors on a single chip will make DNA sensing devices more cost effective. In addition to that, operating them in a parallel fashion will create new potential for integrated microfluidic systems as cheap portable analytical equipment with high throughput. A magnified model image of the single nano-pore with two electrodes while strand of a DNA emerges from it is shown in Figure 2.7.

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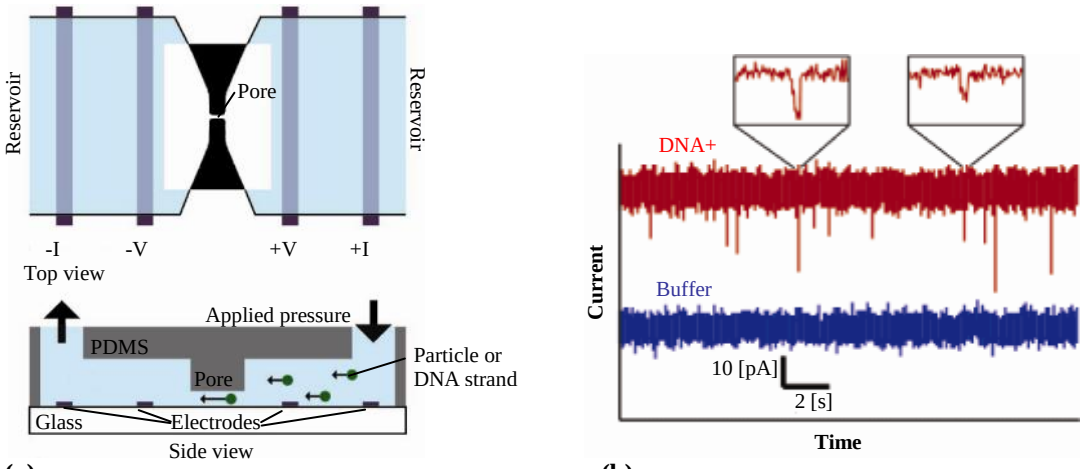

Figure 2.6: (a) Micro Coulter counter with pore fabricated in PDMS [44], (b) DNA strand detection [45].

DNA molecule sensing with nano-meter pore diameter is a new emerging technology utilising the Coulter principle – drops in ionic current amplitude are recorded while the dsDNA[7] molecule translocates through the nano-pore thus blocking the current flow through it. The idea of the device as well as measurement results are shown in Figure 2.8. The concept of the engineered 8 nm diameter pore embedded into graphene[8] membrane separating two Ag/AgCl sensing electrodes was shown by Garaj *et al.* [52].

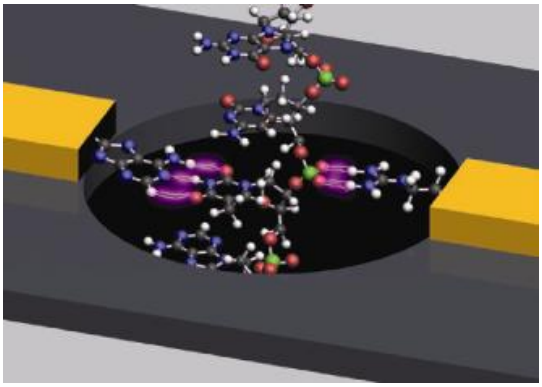

Figure 2.7: The modelled image of a DNA strand emerges from nanopore [50].

[7] Double stranded deoxyribonucleic acid.
[8] Single carbon atom thick planar crystal lattice structure.

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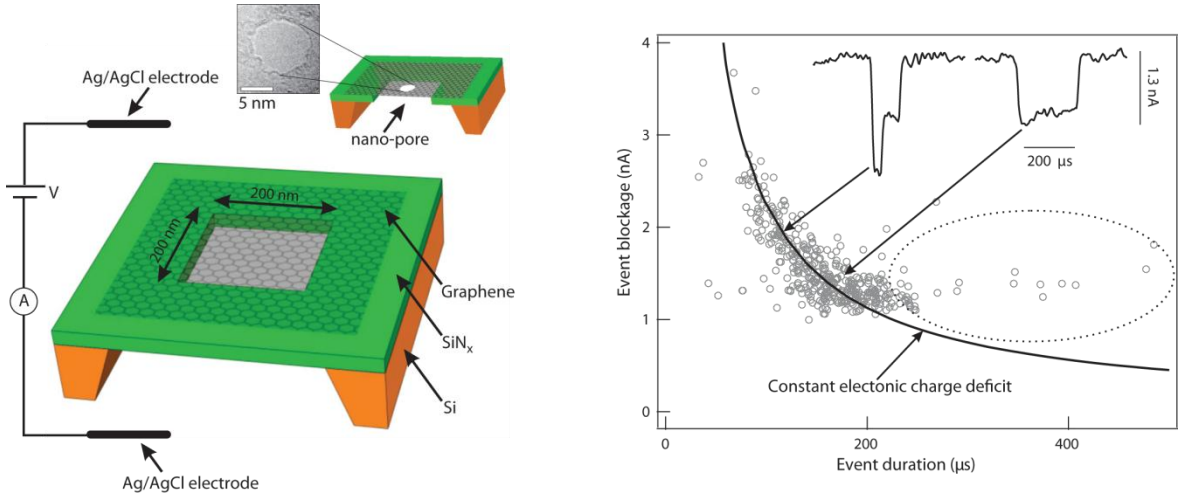
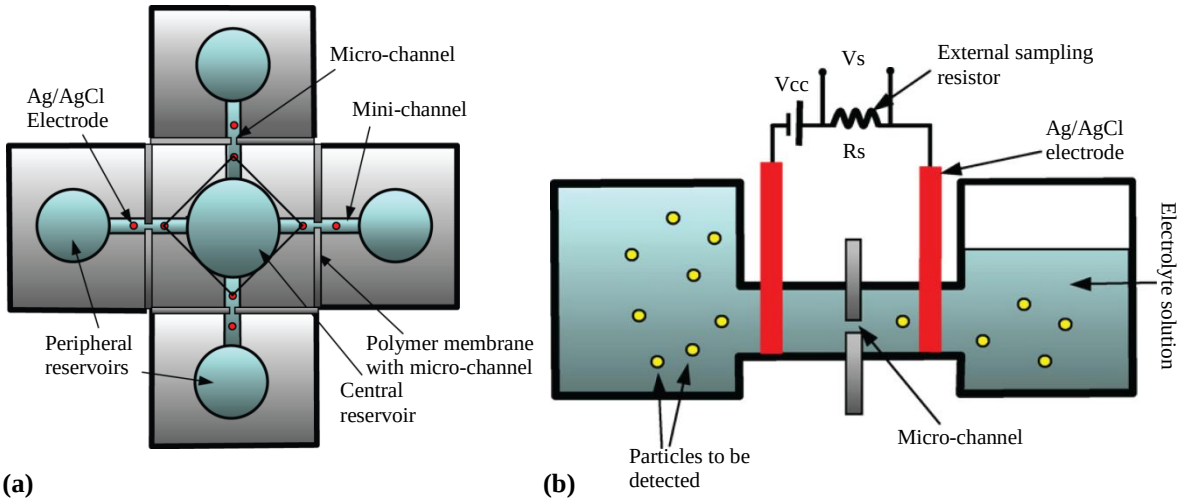


(a) **(b)**

Figure 2.8: The DNA molecule sensing with a thin membrane [52]. (a) The nano-pore embedded into the graphene membrane, (b) Current blocked while DNA molecule passing through the pore.

Important parameters of the micro Coulter counter are its throughput and sensitivity. With the single aperture approach the whole sample needs to pass through a one micrometre (sub-micrometre for single molecule sensing) diameter micro-channel. This requirement decreases the speed of the measurement in a cell culture study. To increase the throughput a multi-aperture device was designed by Jagtiani *et al.* [53, 54]. The device shown in Figure 2.9 (a) was equipped with four sensing micro-apertures made in polymer and was tested with several micro-particle diameters i.e. 20 μm and 40 μm. A single sensing channel with its measurement setup is shown in Figure 2.9 (b). The resistor R_S is an external sampling resistor, the DC voltage V_{CC} is applied to the Ag/AgCl electrodes which are immersed in reservoirs on both sides of the micro-channel. While a microparticle passes through the aperture it displaces electrolyte in micro-channel thus increasing its resistance.



(a) **(b)**

Figure 2.9: (a) Top view of a four micro-channels resistive pulse sensor microparticle counter [54], (b) Schematic of a single channel [54].

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This causes a change in the measured voltage V_S, as shown in Figure 2.10 (a). The magnitude of the voltage pulse shown in Figure 2.10 (b) corresponds to the microparticle size. A similar concept with the sampling resistor and four channel measurement was used by Zhe *et al.* [55].

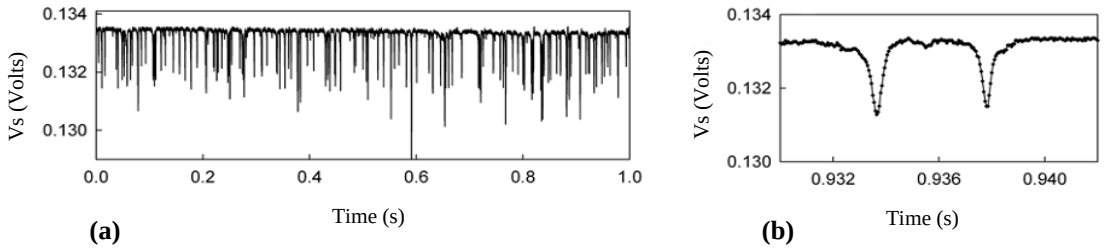

Figure 2.10: (a) The measured voltage trace across one sampling resistor, (b) magnified voltage pulses.

As mentioned before, a Coulter counters' sensitivity can be significantly improved by introducing alternating current sensing method. By performing an AC measurement of the cell subpopulation it is possible to distinguish between cells that are healthy, dead or exposed to toxins via the impedance measured at multiple frequencies [56]. Küttel *et al.* [57] differentiated between healthy and *Babesia bovis*[9] infected bovine erythrocytes using the microfabricated flow cytometer developed by Demierre *et al.* [58]. The measurement results showed that infected red blood cells (RBCs) were clearly differentiated form the uninfected at a frequency of 8.7 MHz whereas the measured impedance in the lower frequency range (10 kHz – 1 MHz) did not show clear differences between infected and healthy RBCs. However the impedance measurement at this frequency range was related to the size and membrane properties of the cells in their experiment. Another device developed by Fuller *et al.* [56] was used to characterise human peripheral blood granulocytes at frequencies ranging from 100 kHz to 10 MHz. Experimental results presented were: a mean radius of 4.1 μm, capacitance of the membrane of 0.9 $\mu F/cm^2$ and cytoplasm conductivity of 0.66 S/m. A single cell analysis with ability to differentiate between the erythrocytes, ghost cells and latex beads was presented by Gawad *et al.* [59]. The impedance was measured using the method illustrated in Figure 2.11 (a) and (b). Two pairs of microelectrodes deposited on the glass substrate measure the micro-channel impedance. The first pair of the electrodes *AD* is used for sensing electric current changes due to a cell passage, while the second pair *DB* measures current passing through the empty cell surrounding media and makes reference measurement. The impedance is recorded over multiple frequencies, ranging from 100 kHz up to 15 MHz. The measured impedance change (Z_{AC} - Z_{BC}) as a cell passes through the micro-channel is shown in Figure 2.11 (b). Moreover, the

[9] An intraerythrocytic protozoan parasite.

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speed of the cell can be calculated, as the distance between the two measurement zones and time t_{tr} between two measured signals (suspension plus cell and suspension only) are known. The measurement results showed that the ghost cells present lower impedance at the high frequency as the healthy cell's interior impedance was similar to the surrounding solution. The reported throughput of the fabricated device is over 100 samples per second (S/s).

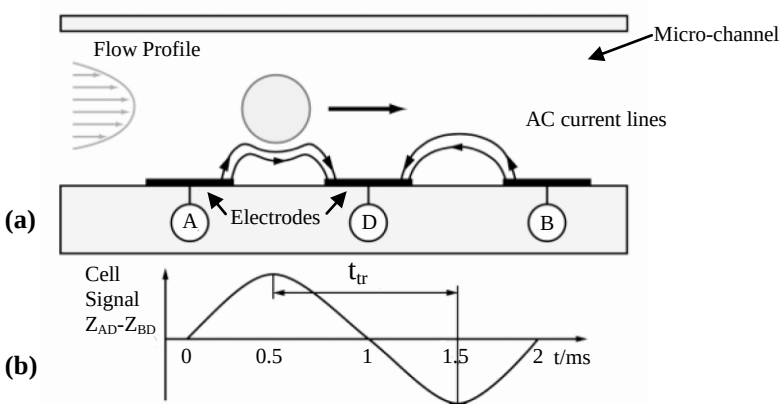

Figure 2.11: (a) Cross-section view of the micro-channel and particle passing over three electrodes (A, B and D), (b) Impedance signal [59].

The differential impedance approach has several advantages such as the impedance of the cell is measured directly against its surrounding media and any uneven drift of the micro-electrodes is corrected [59]. Several designs for microparticle impedance measurement based on the coplanar electrodes (Figure 2.11 (a)) have been done by the other research groups: Wood *et al.* [60], Nieuwenhuis *et al.* [61], Morgan *et al.* [62], Murali *et al.* [63], [64]. Combining the Coulter counter with multiple micro-channel measurement will increase throughput of the entire system. The amplitude modulated Coulter counter with two [65], and four multiplexed microfluidic channels was developed by Jagtiani *et al.* [66]. The simplified equivalent circuit model of the four channel Coulter counter is shown in Figure 2.12 (b). Micro-channels with sensing apertures as well as metal electrodes' layout are shown in Figure 2.12 (a). All of the four channels use the same set of sensing electronics.

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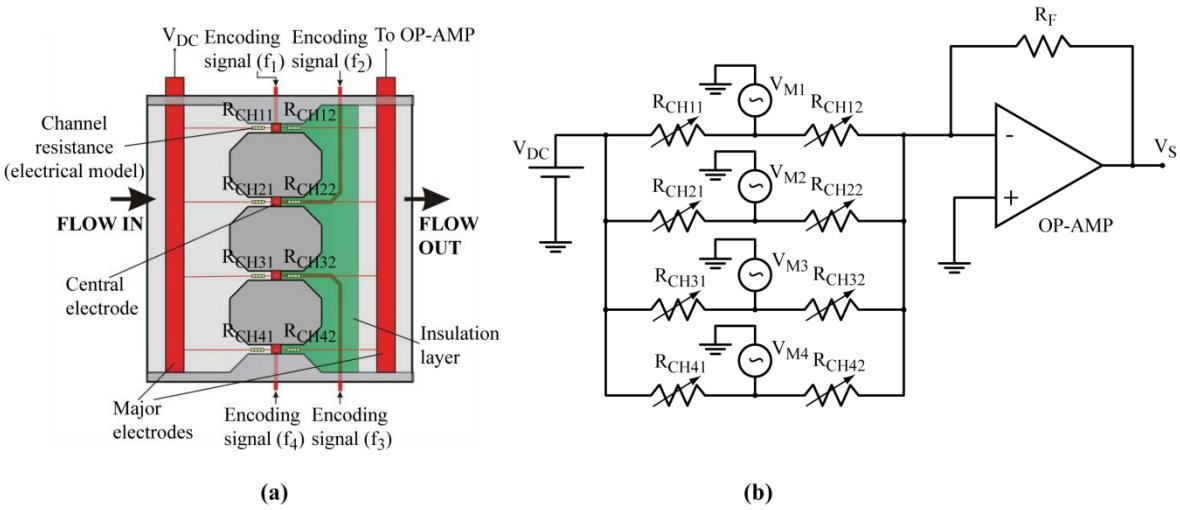

Figure 2.12: (a) Top view of the multichannel microfluidic device [66], (b) Equivalent electrical circuit of the sensor with single set of measurement electronics [66].

The first major electrode supplies DC bias voltage while the second one on the other side of the micro-channel is connected to the inverting input of the summing amplifier with a feedback resistor R_F. The central electrodes are exposed to the solution only in the middle of each channel. These electrodes provide amplitude modulated signals with unique frequency for each of four channels. The central electrode divides each micro-channel into the two parts shown on the equivalent circuit as R_{CH} (with corresponding number of the half channel). The output voltage of the OP-AMP is demodulated to recover the signals from each channel. The recovered output signals for all four channels with changes due to particles passing can be seen in Figure 2.13. Each downward pulse represents one particle passing through the aperture. The relative change in channel's resistance can be calculated from Equation 2.3.

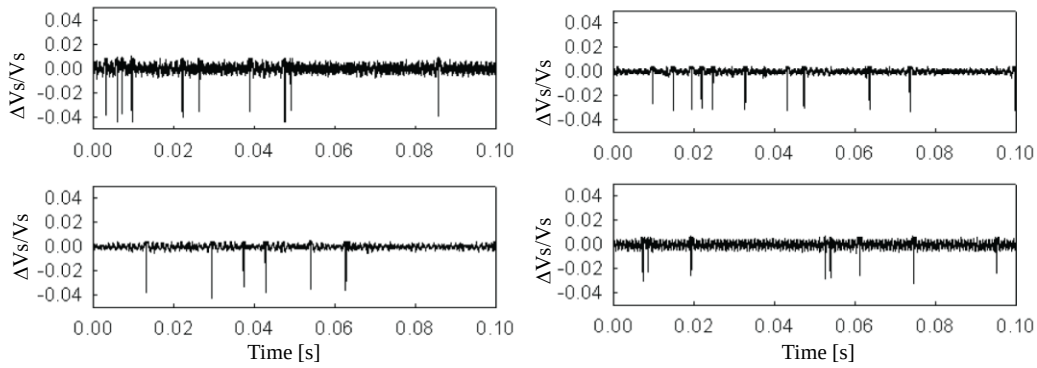

Figure 2.13: Relative voltage change for all the channels while particles passing through [66].

$$\frac{\Delta V_S}{V_S} = \frac{R_{CHi2} - R_{CHi2}'}{R_{CHi2}'} = \left| \frac{\Delta R_{CHi2}}{R_{CHi2}} \right| \tag{2.3}$$

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where: ΔV_S is the voltage change at the output of the OP-AMP due to particle passes in the channel, V_S is the OP-AMP output baseline voltage with empty micro-channel, R_{CHi2}' channel resistance with particle and R_{CHi2} channel resistance without particle in it.

Using the multiplexed multi-aperture Coulter counter increases the throughput whilst minimising the sensing electronics to a single set of instrumentation common for all the channels. The approach provides the foundation for increasing the number of the sensing apertures that will further increase measurement system's throughput.

The circuit developed by Mills *et al.* [67] introduces further improvement to a multi-sensor array impedance readout using a multiplexers to switch between a sensors and read their properties. The multiplexers' on-resistance is not incorporated into the impedance reading of the sensors due to their insertion into a bridge circuit, shown in Figure 2.14. The circuit is designed to measure the impedance of a QCM (quartz crystal microbalance) with a four-terminal approach (Kelvin method). The QCM is located in a feedback loop of an operational amplifier, a change in a voltage drop across the QCM influences directly an output voltage of the op-amp. The current through a QCM is sensed using a differential amplifier connected across a source resistor R_S. Having the current flowing through the QCM and the voltage drop across it, the sensor's impedance can be calculated.

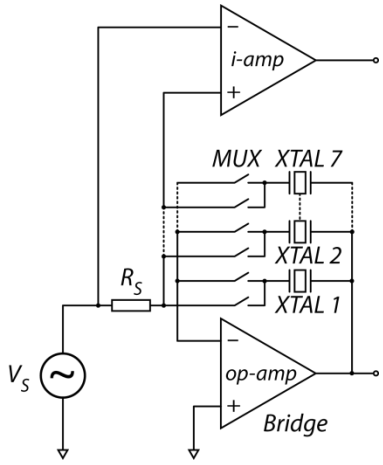

Figure 2.14: Current and voltage measurement technique [67].

2.4 Sensor System on Chip Technology

Commercial semiconductor technology consists of multiple metal layers and active devices (transistors) integrated together as a multilayer structure which enables unprecedented capabilities of integration of both circuitry and various sensing structures on a single silicon

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die. Various microparticle measurement devices have so far been discussed but all of them have got one common feature; each device consists of a single or a multiple sensors measuring the same parameters across all apertures. The electronics industry, and especially very large scale integrated circuit manufacturers, increase the number of embedded devices on a single chip level to decrease a unit cost of the system and increase its manufacturability. The sensor-system-on-chip (SSoC) concept leads the way to the portable low cost medical technology. The Complementary Metal Oxide Semiconductor (CMOS) is the main technology used in SSoC devices manufacturing [10]. In CMOS process there are two basic devices: NMOS (n-type) and PMOS (p-type) field effect transistors. They are used as the basic building blocks to form complex circuits. Both analogue and digital circuits or a mixture called mixed-signal circuits are used. Mixed-signal circuits are ideally suited for SSoC devices where the analogue part of the system is used for an electronic signal (current or voltage) readout from the on chip sensor and digital subsystem for its processing and off-chip transmission [68].

2.4.1 CMOS fabrication

A good understanding of a CMOS process is required to enable design and subsequent post-processing. CMOS microfabrication begins with silicon wafer doping using an n-type or p-type dopants creating either an n- or p-type silicon substrate. There are also twin- and triple-well processes (also called twin- and triple tub processes) where both n- and p-type impurities are implanted onto undoped common substrate to create an n-well, deep n-well and p-well [69, Chapter 2]. To form an n-well a silicon p-type substrate is implanted with donor atoms e.g. phosphorus. Prior the phosphorus atom implantation the substrate is coated with a silicon dioxide to develop a mask with opening (mask window) over a desired location for the n-well. A thin layer of silicon dioxide is then thermally grown over an active area to form a gate oxide ("thermal oxide") which is shown in Figure 2.15 (a). The active devices are isolated by the silicon dioxide layer (field oxide) formed in shallow trenches creating shallow trench isolation (STI). The transistors' gates are patterned by depositing polycrystalline silicon (polysilicon) in the centre of each of the active areas, process is shown in Figure 2.15 (b). Areas designated for drain and source of the NMOS transistor are doped with donor atoms e.g. phosphorus forming heavily doped (n+) regions. To fabricate the PMOS transistor the source and drain regions are doped with acceptors atoms e.g. boron to form (p+) regions. A cross-section through both NMOS and PMOS transistor is shown in Figure 2.15 (c). Both active devices are insulated with thick layer of the silicon dioxide called pre-metal-dielectric (PMD), in which openings are etched to provide contact to gate, source and drain regions. Through these openings a metal (aluminium and copper

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alloys) contacts are introduced to form connection between devices (Figure 2.15 (d)). Metal is deposited on top of the wafer filling the openings in a dielectric layer then is grinded until is flat (damascene process[10]).

In most of the CMOS processes there are multiple metal layers isolated by intra-metal dielectrics (IMD). The multiple metal layer processes may provide additional devices e.g. capacitors (called metal-insulator-metal capacitors) embedded into IMD. A top metal layer is coated with thick dielectric called passivation layer (silicon nitride and silicon oxynitride) to insulate entire CMOS structure from environment contaminants. To perform contacts between CMOS devices and outside circuitry openings in the passivation layer above bond-pads are etched to allow bond-wires to be connected. The CMOS process now offers more than it was originally designed for, not only integrating electronics circuitry but devices capable of measuring/interacting with surrounding environment. For the past few decades there have been many successful approaches to integrate sensors together with the readout a circuitry and a signal processing components on a single silicon dice [10], [68].

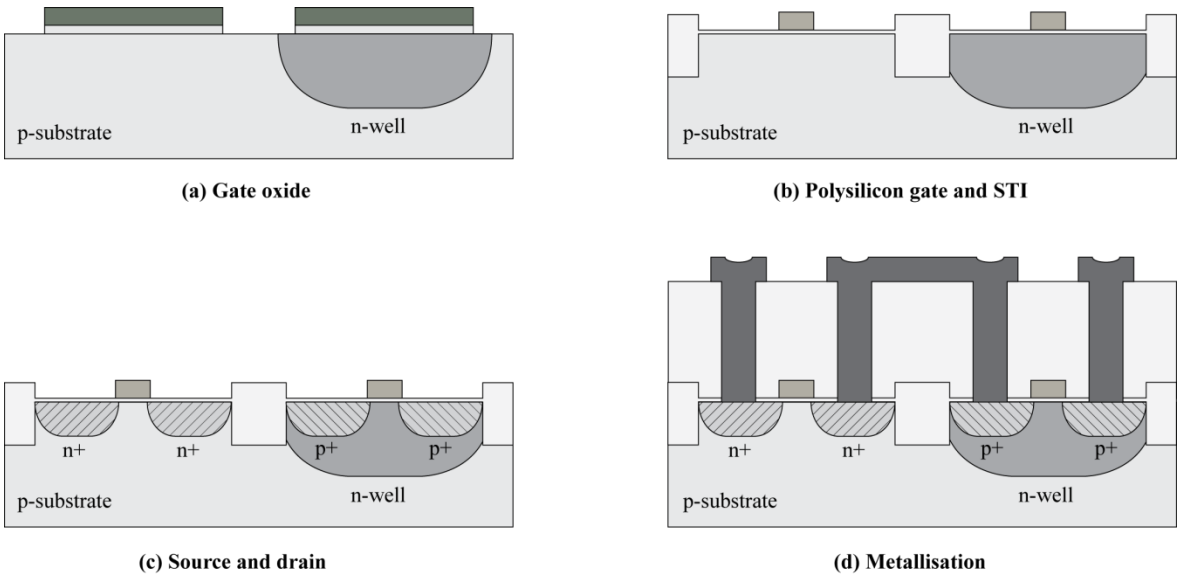

Figure 2.15: Cross-section through a CMOS wafer at various stages while fabrication.

Micro-electro-mechanical-systems (MEMS) are becoming more and more advanced where it is now possible to embed complex 3-D sensors and mechanical structures (e.g. accelerometers, gyroscopes) into silicon chip by conventional CMOS technology. To enable the on-chip sensor operation the silicon dice need to be micro-machined. In general terms MEMS fabrication process can be divided into two basic operations: surface and bulk mi-

[10] A process invented in the city of Damascus to inlay noble metals in swords.

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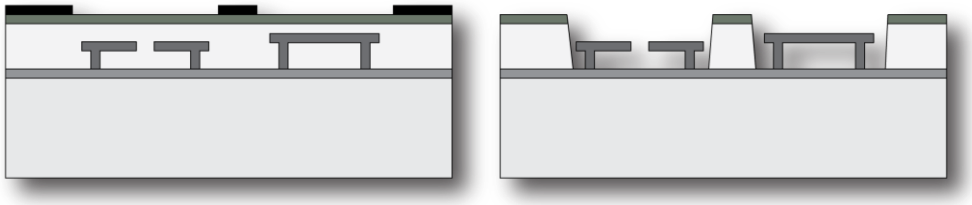
cro-machining. The surface micro-machining metal layers and intra-metal dielectric (IMD) layers are used to develop the sensor structure (Figure 2.16). Both metal and IMD layers can be etched, usually by a deep reactive ion etch (DRIE) utilising various gases in the etch process. By using surface micro-machining techniques in a device post-processing a sensor structure for microparticles or cells differentiation can be developed [70]. As an etch-stop the metal layer is usually used in surface processing. Another method used in surface micromachining is a focused ion beam (FIB) which allows milling the chip surface without applying a resist mask on top of it [71].



(a) Micro-fabricated device **(b) 3D structure released by DRIE**

Figure 2.16: CMOS compatible surface post-processing

The bulk micro-machining process relies on the silicon substrate processing (etching) in desired locations of the chip or entire wafer using the pre-metal-dielectric as the etch stop layer (Figure 2.17). Removing the bulk silicon under sensing structures enables thermal isolation of the sensing structure desirable in thermal imaging sensors. A circuitry embedded into back-end-of-line layers over the etched substrate becomes sensitive to stress variation in a created membrane e.g. MEMS microphones. Combining both MEMS and CMOS technology allows developing various kinds of sensors e.g. chemical and biomedical pH-ISFET based sensors are the brightest example [72], [73].

(a) Isotropic **(b) Anisotropic**

Figure 2.17: CMOS compatible bulk post-processing

Sensor integration in CMOS technology enables miniaturisation and integration of both sensor and readout circuitry on the same silicon dice which in combination with a low

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manufacturing cost and large volume production capabilities makes MEMS technology unique and expanding to various fields, where CMOS sensory system can reveal its potential [10]. In consequence various types of physical properties can be measured by CMOS based sensors:

- **Chemomechnical sensors** typically use a chemically sensitive material (e.g. polymer) deposited in post-fabrication on top of the sensing area whose mass is altered due to absorbed gas molecules, that change is detected by a deflection of a micromechanical cantilever or by a frequency change of a resonating structure as well as by a surface acoustic wave.
- **Thermal sensors** detect change in temperature of an analyte utilising thermocouple as sensing element.
- **Optical sensors** measure a change in light intensity due to photoluminescence generated by a test sample, photo-generated charge changes output current from semiconductor device.
- **Electrochemical sensors** operate on the voltage, current or resistance change due to charge transfer in an ion sensitive interface.
- **Dielectrometric sensors** measure a variation in sensing device capacitance due to dielectric constant change of the analyte.

The output analogue signal produced by the sensor influenced by the analyte need to be measured by a readout electronics circuitry.

Before system-on-chip devices the electronics was provided by an off-chip circuit, usually embedded on a printed circuit board (PCB) level. Integration of both sensor and circuitry on the single chip found its way in a ‘system-on-chip’ concept. Early work carried out by Yeow *et al.* [74] demonstrates integration of a 15 x 16 pH sensor array with readout circuitry. The solid state device was developed and fabricated in a modified CMOS process which required additional CMOS compatible post-processing and was encapsulated by coating the entire chip (except sensing area) with polyimide layer. More advanced SoC device for a gas sensing purpose was developed in 2003 by Hagleitner *et al.*[75]. The solid state device (Figure 2.18 (a)) integrates: chemically sensitive capacitive sensor, calorimetric and temperature sensor integrated together with a readout and signal conditioning circuitry. In addition to that an on-chip analogue to digital conversion was implemented to improve signal-to-noise ratio and take advantage of a robust digital interface to transmit data off-chip. To enable operation of an on-chip sensing structures both surface and bulk

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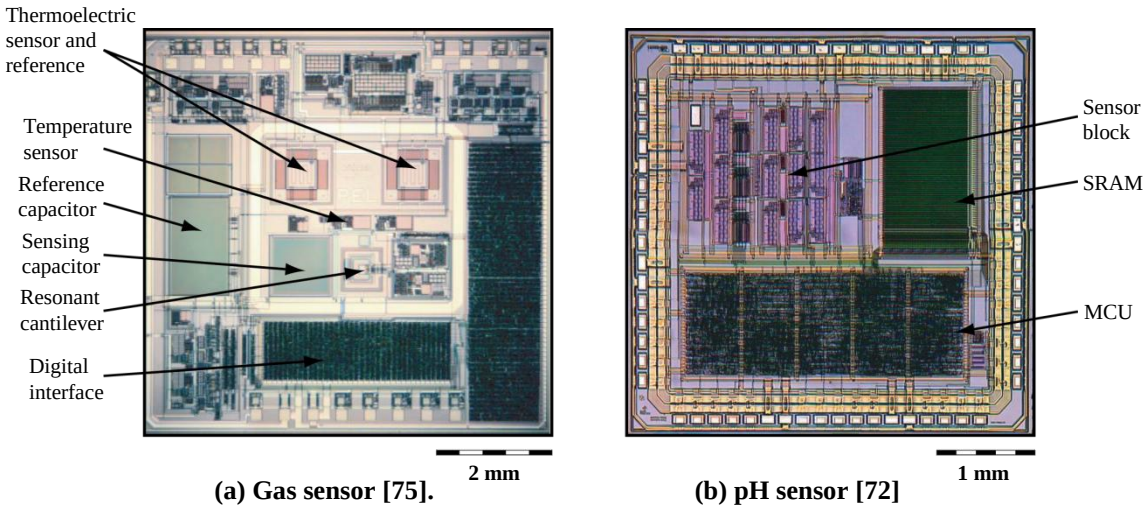
micro-machining techniques were employed in post-fabrication process. A work carried out by Hammond *et al.* [72] shows a complex system-on-chip integrating an ion sensitive field effect transistor (ISFET) based ion sensor and a temperature sensor implemented in unmodified CMOS process, both controlled by an on-chip programmable microcontroller unit (MCU). The system uses differential pH sensing method with temperature stabilisation to reduce both pH sensor's short term drift[11] and temperature influence on pH index reading. An analogue readout signal from a pH sensor converted to digital domain could be stored in on-chip static random access memory (SRAM) or transmitted to an off-chip wireless interface.



(a) Gas sensor [75]. **(b) pH sensor [72]**

Figure 2.18: Microphotographs of two Sensor System on Chip devices.

The example of sensor integration in standard unmodified CMOS technology was demonstrated in 2005 by Milgrew *et al.* [76]. An on-chip ISFET 16 x 16 array was developed for direct extracellular imaging.

The system integrates individually addressable ion sensor array together with a control and readout circuitry. The chip allows to record pH index variation in a close proximity to the sensor array eventually take a 'pH gradient' image of an analyte above the array. It was demonstrated that sensor is capable of monitoring living cell population. However an analogue signal needed to be post-processed by a data acquisition (DAQ) software to reconstruct the pH gradient distribution image of an analyte.

In 2003 a neuron cell activity recoding by a sensor-system-on-chip was presented by Eversmann *et al.* [77]. An array of 128 x 128 capacitance sensing pixels and readout electronics with pixels' mismatch cancelling circuitry was realised in a standard CMOS process. The temperature was controlled by both on-chip resistive temperature sensor and

[11] Occurs in the ISFET due to a dielectric constant gradual change of an electrolyte-insulator-semiconductor interface while exposed to an analyte solution.

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off-chip Peltier element[12] to eliminate environment temperature variation while neural activity recording. Pixels with 7.8 µm x 7.8 µm pitch embedded into matrix 1 mm x 1 mm in size together with interface electronics detects signal of an order of 100 µV to 5 mV peak-to-peak with 2 kilosamples per second per pixel sample rate. The intracellular and extracellular potential from the cell cultured above the array was successfully recorder by the device.

A dielectrometric and potentiometric sensors are widely utilised in sensor-system-on-chip technology due to its compatibility with commercial CMOS processes and utilising fundamental component – complementary-metal-oxide-field-effect-transistor as a principal system building element.

2.5 The Ion Sensitive Field Effect Transistor

The concept and operation of an ion sensitive field effect transistor (ISFET) was first described by Bergveld [78] in 1970. The ion sensing device was based on floating gate metal-oxide-semiconductor-field-effect-transistor (MOSFET) structure however the gate metal connection was intentionally removed exposing gate oxide. Experimental work carried out by Bergveld showed that by applying a voltage between the source and drain while exposing the gate oxide to an analyte solution, the drain current varies with the concentration of sodium chloride (NaCl) in the solution. He found the MOSFET native silicon dioxide (SiO_2) used as the ion-sensing membrane to be sensitive to concentration of sodium (Na^+) as well as hydrogen (H^+) ions in the analyte solution [79] however the ISFET's sensitivity for these two ions differs. Further work carried out by Matsuo *et al.* [80] showed that the silicon dioxide used as a pH sensing layer is limited by its imperfections such as pinholes causing leakage current as well as low pH sensitivity with nonlinear response to ionic concentration. To overcome these limitations a silicon nitride (Si_3N_4) was deposited on top of the thermally grown gate oxide (Figure 2.19). Experimental work showed a superior sensitivity for silicon nitride layer to hydrogen ions together with nearly linear response (close to glass electrode) to ionic concentration as well as very low sensitivity to sodium and potassium ion concentration.

[12] Utilizes Peltier effect – a heat transfer in a p-metal-n type structure due to an electric current flow.

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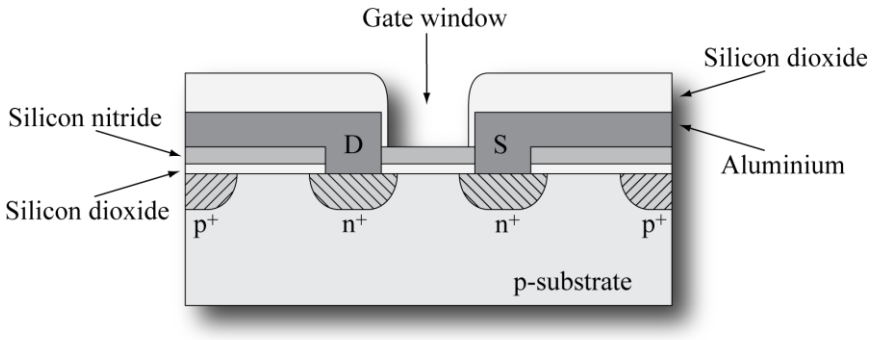

Figure 2.19: Cross-section of the ISFET with silicon nitride sensing layer [81].

However it was experimentally confirmed that the silicon nitride layer pH sensitivity depends on oxygen content in it, and the ISFET sensitivity decreases as the oxygen content in the Si_3N_4 membrane increases. To overcome this problem an aluminium oxide (Al_2O_3) and tantalum pentoxide (Ta_2O_5) films have been used as a gate insulator in the ISFET based pH meter [80]. A number of ion sensing membranes compatible with the ISFET have been investigated. A summary of chemical responses of the various gate insulator materials can be found in Table 2.1. Silicon dioxide has the worst properties in terms of pH sensitivity with nonlinear dependence on ionic variation in an analyte. From the presented data (Table 2.1) it can be seen that the most appropriate pH sensing membrane should be constructed using aluminium oxide or tantalum pentoxide with its superior properties over the silicon nitride. Various oxides have been investigated in conjunction with an ISFET for ion sensing. They include zirconium oxide [82], tin oxide [83], silicon oxynitride [84], [85], and iridium oxide [86]. To decrease the response time to a ionic variation in a solution a platinum [87] as well as titanium nitride [88] has been investigated as the ion sensing layer. CMOS compatible post-processing methods capable of depositing various gate insulator materials for ionic concentration sensitivity enable an ISFET to be an ion selective sensor. However silicon nitride remains the most widely used ion sensing membrane material due to its compatibility with standard semiconductor foundry process where it is used as a passivation layer.

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Gate material	SiO_2	Si_3N_4	Al_2O_3	Ta_2O_5
pH range	4 – 10	1 – 13	1 – 13	1 – 13
pH sensitivity (mV/pH)	25 – 35 (pH > 7) 37 – 48 (pH < 7)	46 – 56	53 – 57	56 – 57
Sensitivity (mV/pH)				
Na^+	30 – 50	5 – 20	2	< 1
K^+	20 – 30	5 – 25	2	< 1
Chemical response time				
(95%) (s)	1	< 0.1	< 0.1	< 0.1
(98%) (min)	undefined	4 – 10	2	1
Long term drift (mV/hr, pH 7)	unstable	1.0	0.1 – 0.2	0.1 – 0.2
Hysteresis (mV)	unstable	3.0	0.8	0.2

Table 2.1: Chemical response of various ISFET gate materials [80].

The clear advantage of the ISFET is its compatibility with standard CMOS process. Early work on combining both the ISFET and CMOS process was mostly focussed on post-processing CMOS devices. In 1988, Bousse *et al.* [89] developed an ISFET using CMOS process steps, the device was coated with a Si_3N_4 layer and used as an ion sensing layer. In addition a silver/silver chloride (Ag/AgCl) reference electrode was deposited around the ISFET on top of the passivation layer. The ISFET integration with readout circuitry in the CMOS process was done by Wong and White in 1989 [90]. In addition to that the differential sensing method was used to cancel out temperature influence on a pH measurement. The device utilised Ta_2O_5 layer as an ion sensitive membrane deposited on top of the SiO_2 gate insulator. In 1999, Bausells *et al.* [91] developed the integrated ISFET in an unmodified commercial CMOS process without the need for post-processing. Process specific a silicon oxynitride passivation acted as the ion sensing layer (Figure 2.20). The ion sensor was integrated together with a readout electronic circuit on a single CMOS chip. A chemical sensor integration using CMOS technology brings novel unprecedented features to disciplines where a rapid response to chemical analyte variation is crucial e.g. blood based medical measurements and DNA sequencing [92]. The another important feature of the ISFET integration with very large scale integrated devices (VLSI) is the ease of design using industry standard electronic design automation (EDA) tools and technologies where the size and cost of a single unit device scales down rapidly together with increasing number of transistors per silicon dice. The concept of a chemical sensing was brought to the point where no longer a single but a multiple chemical sensors are being embedded on a CMOS chip creating ion imaging camera [93].

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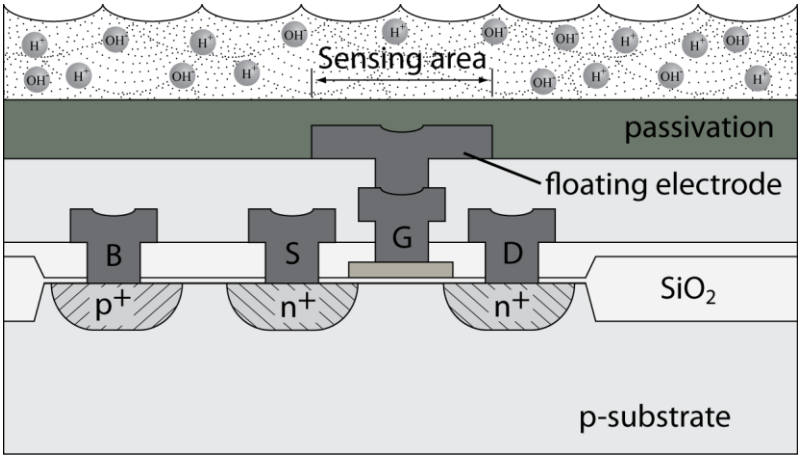

Figure 2.20: Cross-section through an ISFET fabricated using a standard CMOS foundry process [91].

2.5.1 ISFET circuit topologies

An ionic concentration sensing phenomenon using an ISFET relies on surface charge modulation on a sensing membrane. The potential created on an electrolyte-insulator interface depends on the ion specific concentration in the solution. This potential influences the threshold voltage (V_T) of the ISFET which is indirectly measured. To measure the threshold voltage change (ΔV_T) circuitry is required to convert it into a detectable signal. The relationship between the threshold voltage and drain current for a transistor operating in the saturation region (for $V_{GS} > V_T$) is given by:

$$I_D = k' \frac{W}{L} \left(V_{GS} - V_T\right)^2 \tag{2.4}$$

where *k'* is a process-dependent constant, *W* is the gate width, *L* is the gate length, V_{GS} and V_T are gate-source and threshold voltages respectively. The ISFET requires an external gate bias which is applied by a reference electrode immersed in an analyte solution (Figure 2.21). It is very important to keep the analyte potential constant while performing the threshold voltage measurement however in the beginning of the ISFET usage it was stated by Bergveld [79] that there is no need for the reference electrode. Instead of the reference electrode he used a feedback circuit to control the bulk voltage of the ISFET and maintain a fixed drain current. This approach assumes that there is no leakage current from the drain and source terminals and the insulation between the analyte and the ion sensing device is ideal. In reality there is a leakage current in the thin SiO_2 sensing membrane due to its imperfections such as pin-holes which has been described by Matsuo and Esashi [80]. They suggested that using Si_3N_4 as the gate material introduces a significant improvement over a SiO_2 membrane by reducing the leakage current however the oxygen content in Si_3N_4 worsens the overall ISFET sensitivity. For this reason, all of the following ISFET based

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ion sensors include the reference electrode to keep the electrolyte at a constant and well defined potential. The constant drain current of the ISFET can be maintained if V_{GS} *(*=V_G - V_S*)* is fixed. In addition to that V_G is fixed by a constant potential applied to the reference electrode. In consequence as V_T changes with I_D held constant, V_S must change by an equal and opposite amount. This methodology was adopted by Matsuo and Wise [81] to fabricate a needle-shaped probe for a bio-potential recording. The probe consisted of an ISFET and a MOSFET, both with identical geometries. The ISFET was configured as a source-follower and the MOSFET was utilised as a constant current sink operating in the saturation region (Figure 2.21). A gate potential was fixed by a saturated calomel reference electrode. The source-follower configuration was used by Bousse *et al.* [89], where the silver/silver chloride reference electrode was deposited in a close proximity to a sensing membrane on the same chip. Utilising (Equation 2.4) the source-follower, the output voltage V_{OUT} of the measurement circuit was given by:

$$V_{OUT} = V_G - V_T - \sqrt{\frac{I_D L}{k'W}} \tag{2.5}$$

This circuit configuration has two disadvantages; firstly the output impedance is dependent on the current through the source follower and the ratio of *W/L* of the ISFET. Thus it was needed to enlarge this ratio to match current through the source follower and produce the correct output impedance. Secondly this circuit was influenced by the body effect[13] limiting the input/output slope of the source follower, hence reducing indication of the pH sensitivity of the ISFET.

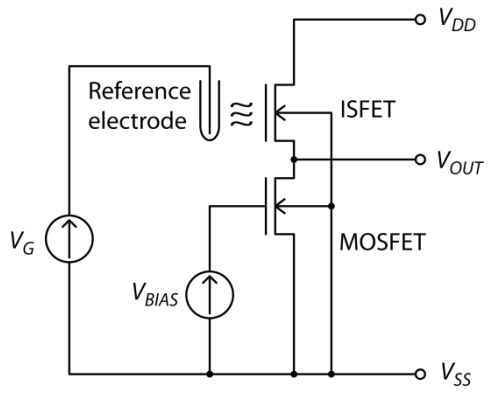

Figure 2.21: Circuit diagram of an ISFET in source follower configuration [81].

These disadvantages were overcome by designing a circuit topology with a source-and-drain follower [94]. This topology can be used in conjunction with an ISFET operating in

[13] When a potential difference between a source and a bulk increases, the threshold voltage increases thus a larger gate-source potential is required to keep a surface of an inversion layer inverted.

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the linear as well as in the saturation regime. The drain current of the MOSFET operating in the linear region is given by:

$$I_D = k' \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{{V_{DS}}^2}{2} \right] \tag{2.6}$$

where V_{DS} is a drain-source voltage. In this region, it is essential to keep both potentials: V_{GS} and V_{DS} constant to ensure the ISFET drain current is fixed. The measured value of V_S determines directly the change in the ISFET threshold voltage due to an ionic variation in an electrolyte solution. The first ISFET combined with the source-and-drain follower circuit was described by Bergveld [95] in 1981, which utilised a complex instrumentation amplifier topology to maintain constant ISFET's drain current at a fixed drain-source voltage. A simpler source-and-drain circuit topology was proposed by Ravezzi and Conci [96] in 1998. The drain-source voltage of the ISFET was kept constant by two unity-gain operational amplifiers A_1 and A_2, which maintain the voltage drop across a resistor R_{DS} equal to the voltage drop across the drain-source terminals of the ISFET (Figure 2.22). A constant ISFET drain current was maintained by a current sink while the constant current through the R_{DS} was fixed by a current source. The unity-gain operational amplifier A_3 was used as a buffer to de-couple the bias circuit from the output terminal and maintain low output impedance.

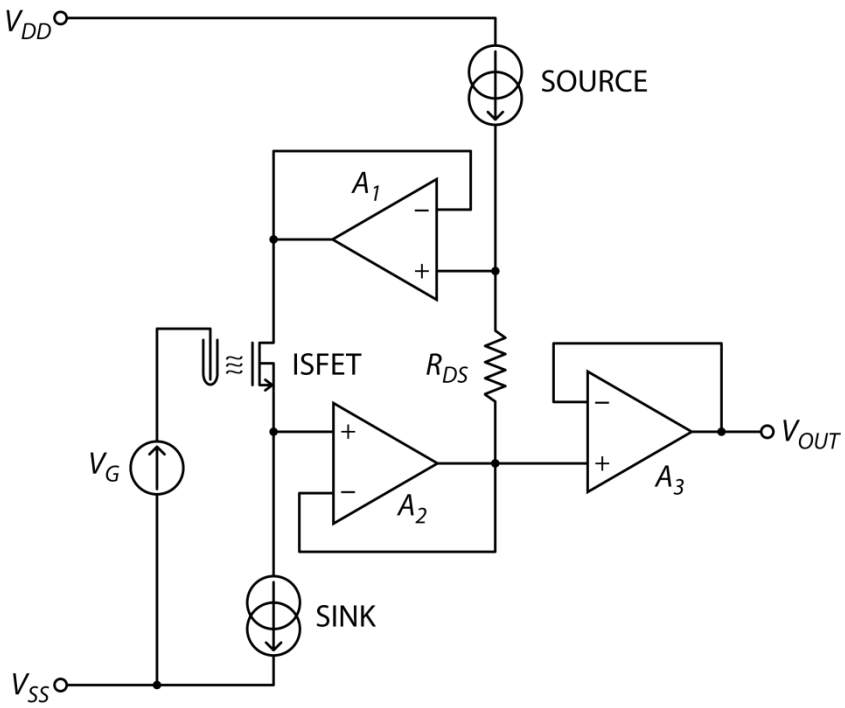

Figure 2.22: Source-and-drain follower circuit diagram [96].

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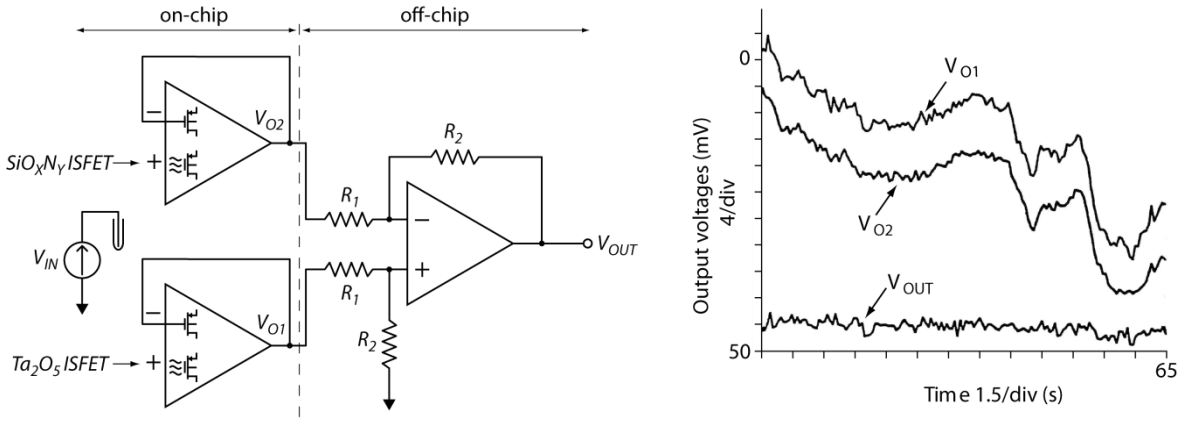
In order to develop a practical micro sensor for pH measurement it is required to integrate the ISFET, the bias-readout circuitry, and the miniaturised reference electrode on a single chip. That need was addressed by Wong and White [90] in 1989. They implemented differential ISFET circuitry together with an on-chip quasi reference electrode (qRE).

The differential measurement was done between two ISFETs with different sensing membranes (Figure 2.23). A tantalum pentoxide layer was photolithographically deposited on the first ISFET gate and a silicon oxynitride layer was developed by oxidising a silicon nitride layer in a dry-oxygen atmosphere at 950 ^{O}C to develop a sensing membrane on the second ISFET gate. To cancel out temperature sensitivity each ISFET was geometrically matched with a MOSFET at the differential input stage of a CMOS operational amplifier. An electrolyte potential was kept constant by a qRE made from a noble metal (Au/Cr). However the qRE/electrolyte interface potential is electrolyte-composition (pH) dependent. This potential appears as a common signal for both ISFETs thus being rejected by means of the differential amplifier circuit as a common mode signal. Current flowing through both ISFET-MOSFET pairs was kept constant by feedback added to control the gate of the MOSFETs in each pair. The change in threshold voltage of the ISFET as the electrolyte pH varied influenced its gate voltage which was tracked by the gate voltage of the corresponding MOSFET thus influencing an operational amplifier output signal. The output terminals from the two operational amplifiers were interfaced with an off-chip differential amplifier. In operation the circuit delivered an electrochemical response of 40–43 mV/pH. The differential pH sensing approach demonstrated a common-mode rejection to ambient light and noise form electrolyte as well as off-chip reference electrode elimination.



(a) Circuit diagram **(b) Output voltage**

Figure 2.23: Block diagram and output voltage of the differential ISFET semsing circuit [90].

Work carried out by Wilhelm *et al.* [84] demonstrated the differential pH sensing methodology using the same sensing membranes – Ta_2O_5 and SiO_XN_Y for two ISFETs respec-

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tively. However the results revealed a response of 45.8 mV/pH for Ta_2O_5 and 39.9 mV/pH for SiO_XN_Y with low differential sensitivity of -5.9 mV/pH. The low differential electrochemical response of the circuit was linked to oxygen content in SiO_XN_Y layer. The other approach to the differential sensing used by Palán *et al.* [97] utilised two source-and-drain follower circuits. This differential system consisted of two ISFETs with Si_3N_4 and SiO_2 sensing membranes respectively, and a platinum qRE. A further advancement to the differential pH sensing technique was introduced by Hammond *et al.* [72] who used two ISFETs with a common Si_3N_4 sensing membrane. One of the sensing electrodes was photolithographically coated with an ion blocking PVC-based membrane thereby realising an ion insensitive FET or reference FET (REFET). The entire ion sensing system was implemented on a single CMOS chip, however due to a difference in drift characteristic between the ISFET and REFET which affected pH measurement, another drift compensation mechanism was implemented by real-time data processing in an on-chip microcontroller.

2.6 Summary

The cell and microparticle measurement have been realised by both optical and electrical methods as well as combination of these two. The current leading method in a portable application can be assigned to an electrical sensing zone which poses a potential for further miniaturisation and parallelisation to increase sample throughput. However implementing a microfluidic device in a commercial CMOS process is not trivial due to the complex post-processing required. The brief introduction to both front and back-side post-processing was provided in this chapter to highlight techniques and present CMOS post-processing capabilities. Further advancements in CMOS based MEMS have been highlighted by identifying CMOS compatible sensors i.e. ion sensors, which can be integrated on a single silicon die to develop a sensor-system-on-chip for single microparticle analysis. The ISFET based ion sensor has a major advantage in its compatibility with commercial CMOS processes however there are limitations i.e. drift and nonlinear electrochemical response which can be overcame by both post-processing and signal conditioning. The theory of electrical microparticle sensing and the ISFET based ion sensor operation will be provided in a subsequent chapter.

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3 Theory

3.1 Introduction

The previous chapter introduced the background literature relevant to the sensor-system-on-chip design and development. This chapter introduces the theory of the single cell impedance based cytometry as well as the ion-sensitive-field-effect-transistor based pH measurement. It starts by describing the electrical model of a cell used in the capacitive cytometry, and then explains the metal electrode-electrolyte interactions stated by the electrical double layer. Then, the "site–binding" model explains the mechanism of the electrolyte-insulator-semiconductor interface potential development responsible for the difference in pH response of the silicon dioxide and silicon nitride used in the ISFET based sensor. Finally the Coulter counter sensor is briefly outlined.

3.2 Cell's Equivalent Circuit Model

A biological cell is the basic functional unit of each living organism, thus observing its functions and actions is of fundamental importance for biomedical and clinical applications. Cellular analysis requires a multi-parametric approach, including counting, manipulation (focussing, trapping, sorting and rotating), identification (labelling) and membrane measurement (thickness, permeability, ion exchange channels) of cells [7]. Traditional techniques used in a flow cytometry are well established for analysis of a cells population where measured parameters are averaged over the entire population. However when observing individual cells, the population averaged information becomes inaccurate. Insight into the individual cell characteristic and behaviour allows differentiation of each cell in the entire population. Using electrical methods the individual cells can be identified on the basis of discrepancies in volume and dielectric properties. Electrical techniques are advantageous where non-invasive and label-free differentiation plays a major role in the cells characterisation. The electrical impedance[14] method measures the AC electrical properties of cells (and a suspension medium) from which the dielectric properties of its components can be identified. The dielectric properties of particles and cells in a suspension medium are defined by Maxwell's mixture theory [98]; it describes the complex permittivity of the suspension medium and the particle suspended in it. Shelled-models based on Maxwell's mixture theory have been utilised in an analysis of the dielectric particles in the suspension medium [99, 100] and the cell's impedance measurement [101, 102]. A biological cell sus-

[14] The ratio of voltage to current passing through the device under test (DUT).

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pended in a medium is described by the single-shelled spherical model as shown in Figure 3.1. Each component of this model has its own distinct electrical properties describing counterparts of the biological cell and suspension medium. The complex permittivity of this model is given by Equation 3.1 [7].

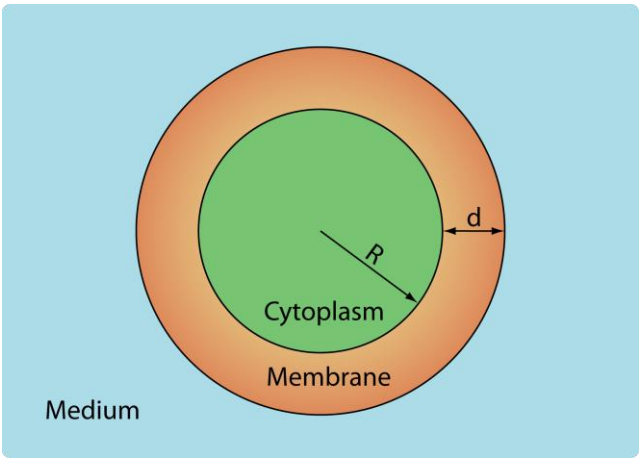

Figure 3.1: Single-shell spherical model of the cell [100].

$$\tilde{\varepsilon}_{mdl} = \tilde{\varepsilon}_m \frac{1+2\varphi\tilde{f}_{CM}}{1-\varphi\tilde{f}_{CM}} \tag{3.1}$$

and,

$$\tilde{f}_{CM} = \frac{\tilde{\varepsilon}_c - \tilde{\varepsilon}_m}{\tilde{\varepsilon}_c + 2\tilde{\varepsilon}_m} \tag{3.1a}$$

where: $\tilde{\varepsilon} = \varepsilon - j\sigma/\omega$ is the complex permittivity, $j^2 = -1$, ω is the angular frequency, $\tilde{f}_{CM}$ is the Clausius-Mossotti factor and $\varphi = (2d^3)/(3D^2L)$ is the volume fraction within the fluidic channel with diameter D and length L. The indexes "c" and "m" correspond to the cell and the suspension medium respectively, $\tilde{\varepsilon}_c$ is the cell's complex permittivity which is a function of the dielectric properties of the membrane and the cytoplasm.

The complex permittivity of the cell is given by [7]:

$$\tilde{\varepsilon}_c = \tilde{\varepsilon}_{mem} \frac{\gamma^3 + 2\left(\dfrac{\tilde{\varepsilon}_i - \tilde{\varepsilon}_{mem}}{\tilde{\varepsilon}_i + 2\tilde{\varepsilon}_{mem}}\right)}{\gamma^3 - \left(\dfrac{\tilde{\varepsilon}_i - \tilde{\varepsilon}_{mem}}{\tilde{\varepsilon}_i + 2\tilde{\varepsilon}_{mem}}\right)} \tag{3.2}$$

with,

$$\gamma = \frac{R+d}{R} \tag{3.2a}$$

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where $\tilde{\varepsilon}_{mem}$ is the complex permittivity of the membrane, $\tilde{\varepsilon}_i$ is the complex permittivity of the cytoplasm, R and d are the inner radius and membrane thickness of the cell respectively.

The relation of a model's complex impedance to its complex permittivity is given by:

$$\tilde{Z}_{mdl} = \frac{1}{j\omega\tilde{\varepsilon}_{mdl}G} \tag{3.3}$$

where G is a geometric constant (ratio of the area of the electrodes, to the distance between them). The geometry (layout) of measurement microelectrodes becomes an important factor when performing single cell analysis and must encompass the influence of a non-uniform electric field between the two electrodes. The electric field non-uniformity occurs due to the effect of a divergent (fringing) field.

To identify the particular components of the cell's model an equivalent electrical circuit analogy is often used. The simplified equivalent circuit model developed by Foster and Schwan [103] approximates the cell to a resistor (R_i) which is the analogue of the cytoplasm, connected in series with a capacitor (C_{mem}) – the analogue of the membrane (Figure 3.2). The suspending medium is modelled by a resistor (R_m) and a capacitor (C_m). The electrical properties of the membrane and the cytoplasm for the simplified equivalent circuit are described by Equations 3.4 and 3.5.

$$C_{mem} = \frac{9\varphi R C_{mem,0}}{4} G \tag{3.4}$$

where $C_{mem,0} = \varepsilon_{mem} / d$ is the specific membrane capacitance per unit area.

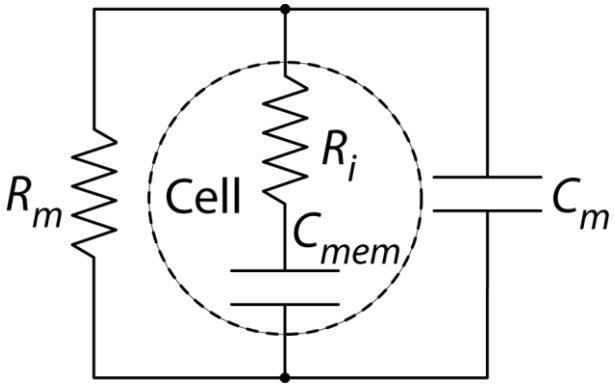

Figure 3.2: Simplified equivalent circuit model of a cell in a suspension medium [7].

$$R_i = \frac{4\left(\frac{1}{2\sigma_m} + \frac{1}{\sigma_i}\right)}{9\varphi G} \tag{3.5}$$

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where σ_m and σ_i are the conductivities of the suspending medium and cytoplasm respectively. The suspending medium is described by Equations 3.6 and 3.7.

$$R_m = \frac{1}{\sigma_m(1-3\varphi/2)G} \tag{3.6}$$

$$C_m = \varepsilon_\infty G \tag{3.7}$$

The limiting high frequency permittivity (ε_∞) of the suspension medium and is given by:

$$\varepsilon_\infty \cong \varepsilon_m\left[1-3\varphi\frac{\varepsilon_m-\varepsilon_i}{2\varepsilon_m+\varepsilon_i}\right] \tag{3.8}$$

where ε_m and ε_i are the permittivities of suspension medium and cytoplasm respectively.

The simplified equivalent circuit model of a cell in suspension medium has been applied to a single cell impedance measurement by Gawad *et al*. [101] and Morgan *et al.* [99]. This model however doesn't take into account a cell's membrane conductance and a cytoplasm capacitance which becomes important during cell membrane electroporation[15] [104, 105] and cell lysis[16] [11, 106]. Additional components need to be added to the equivalent circuit to include the membrane resistance and the cytoplasm capacitance [107]. A complete equivalent circuit model is shown in Figure 3.3. The electrical properties of the membrane (R'_{mem}, C'_{mem}), cytoplasm (R'_i, C'_i) and the suspension medium (R'_m, C'_m) for the complete equivalent circuit are described by Equations: 3.9, 3.10, 3.11 and 3.12.

$$R'_{mem} = \frac{1}{G}\left[\frac{\tau_1+\tau_2}{\Delta\varepsilon_1+\Delta\varepsilon_2} - \frac{1}{k_2+k_3} - \frac{\tau_1\tau_2(k_2+k_3)}{(\Delta\varepsilon_1+\Delta\varepsilon_2)^2}\right] \tag{3.9}$$

where τ_1, τ_2 are the characteristic relaxation time constants, coefficients k_2, k_3 are equal to the dielectric dispersion of each characteristic relaxation time constant [100], G is the geometric constant and $\Delta\varepsilon_1 = k_2\tau_1$, $\Delta\varepsilon_2 = k_3\tau_2$ are the dielectric dispersions of each characteristic relaxation time constant [100].

The suspending medium is described by Equations 3.13 and 3.14 [7].

$$C'_{mem} = \frac{\tau_1\tau_2(k_2+k_3)}{(\Delta\varepsilon_1+\Delta\varepsilon_2)R'_{mem}} \tag{3.10}$$

$$R'_i = \frac{1}{(k_2+k_3)G} \tag{3.11}$$

[15] An increase in a cell plasma membrane conductivity and permeability by external electrical field.
[16] Breaking down of the cell integrity, usually by an osmotic mechanism.

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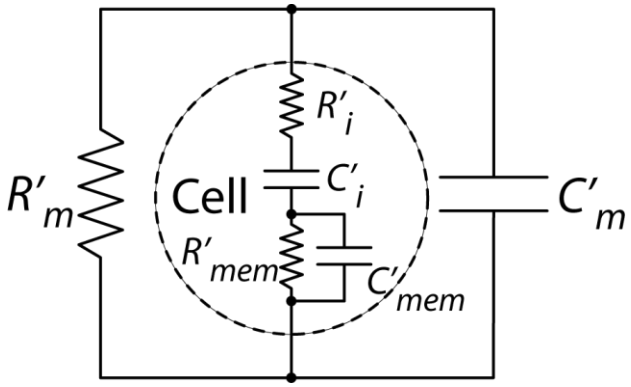

Figure 3.3: Complete equivalent circuit model of a cell in a suspension medium [107].

$$C'_i = (\Delta\varepsilon_1 + \Delta\varepsilon_2)G \tag{3.12}$$

$$R'_m = \frac{1}{\sigma_0 G} \tag{3.13}$$

$$C'_m = \varepsilon'_\infty G \tag{3.14}$$

where σ_0 is the limiting low frequency conductivity of the suspension medium and ε'_∞ is the limiting high frequency permittivity of the suspension medium.

Using Maxwell's mixture theory it is possible to describe the dielectric properties of the single-shelled particle, or the biological cell immersed in a suspension medium, and correlate the particle, or the cell, with the corresponding equivalent circuit model. However to perform an electrochemical measurement, the phenomena occurring between an analyte and a measurement microelectrode needs to be taken into account, thus electrode-electrolyte interaction theory is introduced.

3.3 Electrode-Electrolyte Interface

3.3.1 Electrical double layer

The interface region between a two physically different environments, for example between a solid and a liquid, has unique features, one of which is a potential development across these two phases[17]. The metal electrode/electrolyte junction is an example of such an interface. When a metal or an insulator electrode is immersed in an analyte solution, a potential difference is formed across the interface. A reason for this is the charge transfer between the two phases. The charge separation due to electron transfer will stop when electroneutrality is restored and opposing charged species in both phases are aligned; this will establish the potential difference across the boundary. Arrangement of charged species

[17] A phase is a homogenous part of a heterogeneous structure that is separated by a discrete boundary e.g. soil and water.

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i.e. ions and molecules across the interface region is termed as the electrical double layer (EDL) [108, Chapter 20]. The EDL concept was developed by Helmholtz in the late 19th century. The electrified interface between the electrode and the electrolyte solution consists of several distinct layers [109] which can be seen in Figure 3.4.

The innermost layer is a hydration sheath that is composed of a monolayer of water molecules. Water molecules are adsorbed on the electrode surface by an electrostatic means. The water dipoles orientate themselves in accordance to the surface charges present at the electrode. The electrostatic interaction between a charged electrode and the water dipoles plays an important role in a specific ion adsorption at the electrode surface. A specific ion adsorption at the surface of the electrode occurs when unhydrated counterions are found within the hydration sheath. The location of the adsorbed unhydrated ion plane is termed the inner Helmholtz plane (IHP). These unhydrated ions are adsorbed to the electrode surface via chemical means. Electrostatic forces originating from charges in the electrode do not affect these ions, thus ions charged coherently to the electrode charge can be found in the IHP.

The next layer behind the hydration sheath is defined by a locus of hydrated ions. Since the example electrode depicted in Figure 3.4 is negatively charged (cathode), the hydrated ion layer is populated by cations with appropriate countercharges. The position of this layer defines the outer limit of the molecular capacitor called the outer Helmholtz plane (OHP). According to the Helmholtz-Perin model [108, Chapter 20] the molecular capacitor plates, created by the charged electrode surface and the OHP, stays in equilibrium due to an opposing charge arrangement where the net transfer of charge across this interface is zero and the capacitance associated with it is expressed by Equation 3.15, where ε_0 and ε_r are permittivities of free space and the electrolyte respectively, A is the total surface area of the overlapping electrode and OHP and d is the distance between these two electrodes.

$$C_H = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{3.15}$$

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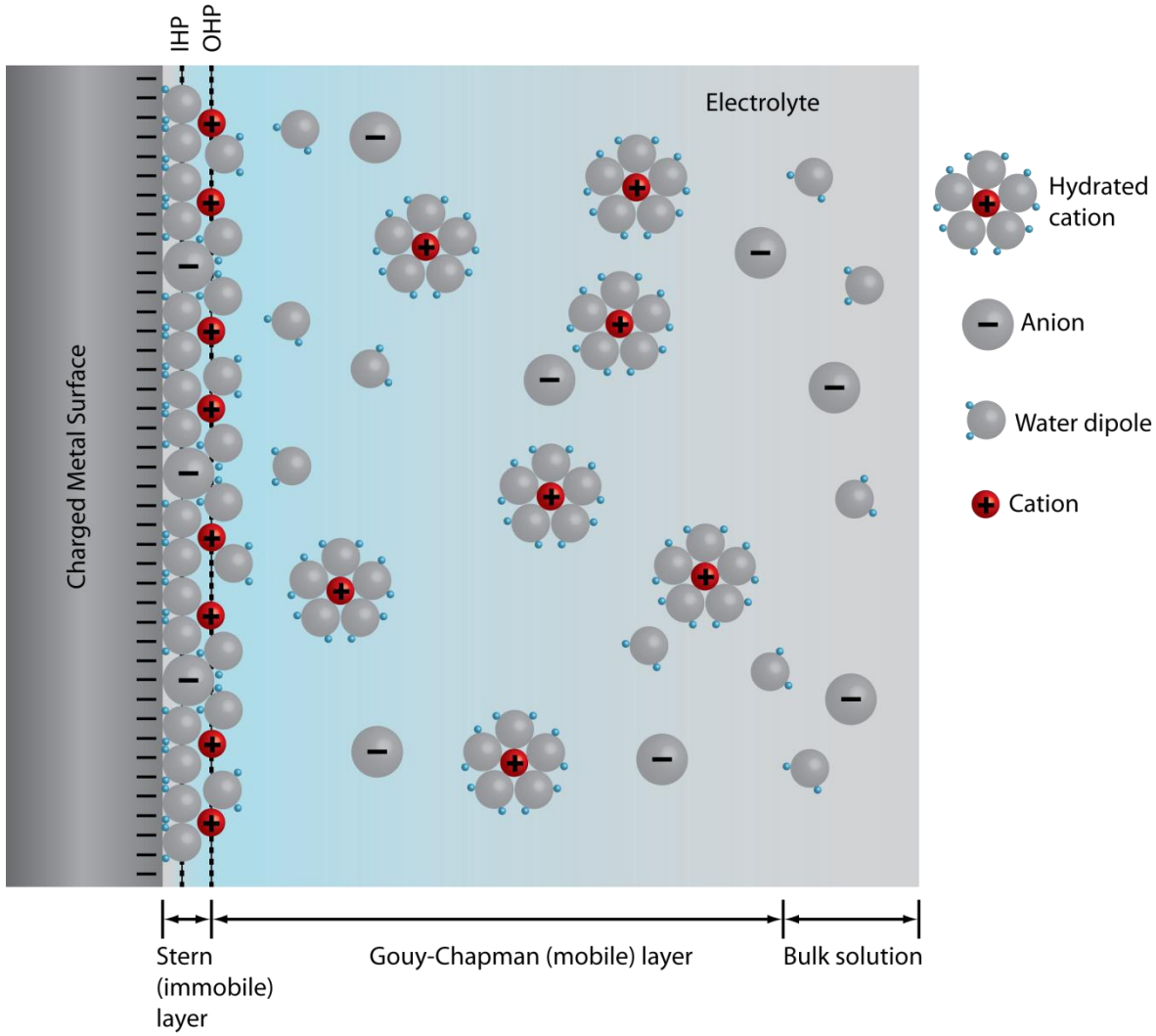

Figure 3.4: Electrical double layer at the metal-electrolyte interface.

The interaction between the OHP and the electrode involves long-ranged electrostatic forces, thus adsorption of ions at that plane doesn't depend on their chemical properties (non-specific ion adsorption). The IHP and OHP together compose a Stern layer which is also termed the immobile layer. The OHP is a demarcation line between the Stern and a Gouy-Chapman (diffuse) layer [109]. The diffuse layer extends from the OHP into a bulk electrolyte. Ions dispersed in this layer are defined as a diffuse cloud, where the charges are unevenly distributed. The high concentration of charges distributed near the OHP decreases exponentially as the distance from the electrode surface increases.

The voltage drop across the diffuse cloud has an exponential decay profile given by

$$V(x) = V_0 \exp^{(-x/L_D)} \tag{3.16}$$

where $V(x)$ is the potential at distance x from the charged surface, V_0 is the potential at the charged surface at $x=0$ and L_D is the *Debye length*[18].

[18] Characterizes spatial decay of the potential thus defines a characteristic thickness of the diffuse layer.

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The differential capacitance per unit area (F/m^2) of the Gouy-Chapman layer is given by:

$$C_G = \underbrace{\frac{\varepsilon_0 \varepsilon_r A}{L_D}}_{first term} \underbrace{\cosh\left(\frac{zV_0}{2V_t}\right)}_{second\ term} \tag{3.17}$$

where the *first term* is the capacitance per unit area of the molecular (linear) capacitor, the nonlinear *second term* (represented by a hyperbolic cosine) accounts for the effect of mobile charges in the diffuse layer, V_t is the thermal voltage and z is the valence of the ion species.

The total interfacial capacitance derived by Stern [110] combines both Helmholtz and Gouy-Chapman capacitors connected in series (Equation 3.18). It results in a linear potential decrease in a region between the electrode surface and the OHP, and a near exponential voltage drop in the region between OHP and a bulk solution.

$$\frac{1}{C_I} = \frac{1}{C_H} + \frac{1}{C_G} \tag{3.18}$$

The change in the interfacial capacitance with the electrolyte potential variation can be seen in Figure 3.5. As the ionic concentration in the electrolyte increases, C_G also increases, thus C_I approaches a fixed value of C_H. The same applies to the electrode potential changes, as it moves away from a potential at point of zero charge[19] (V_{pzc}), C_I increases to C_H (according to Equation 3.17), where the V_{pzc} is defined as a difference between the actual electrode potential (V_{el}) and the potential where the electrode's surface charge density is zero ($V_{\sigma_0=0}$). This is due to a dominant effect of the electric field across the interface over the thermal effect of the electrolyte solution ($V_0 > V_t$). Contrary to this, as the ionic concentration in the electrolyte decreases the value of C_I will tend towards the value of C_G ($V_0 > V_t$), shown in Figure 3.5.

[19] Point of zero charge (pzc) is a condition when the electrode surface charge density is zero.

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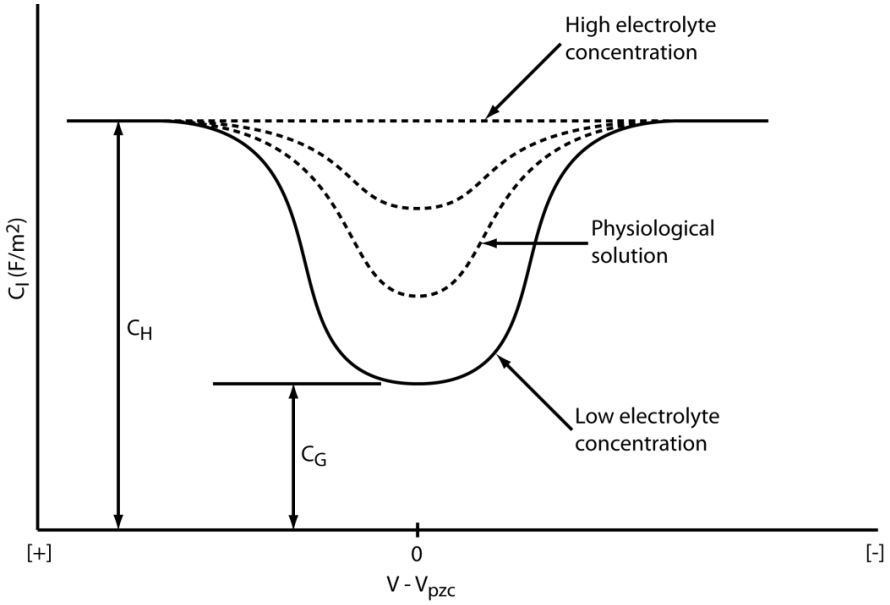

Figure 3.5: The expected behaviour of C_I according to the electrolyte concentration and the electrode potential change [111].

When the metal electrode is in contact with an electrolyte solution a net charge transfer takes place between these two phases, due to an electrochemical reaction, until an equilibrium state is reached (net flow is zero). The heterogeneous transfer of net electrons across the electrode-electrolyte interface defines Faradaic impedance, were the change of the electrode (equilibrium) potential value due to electrons transfer is termed polarisation. A difference between the V_{el} and an interface equilibrium potential value (V_{eq}) is termed as an overpotential (η). η is a measure of an electrochemical reaction's influence on the interface (Equation 3.19).

$$\eta = V_{el} - V_{eq} \tag{3.19}$$

While the potential is applied across the interface the net current will flow. The relation between the η and a net current density J is given by

$$J = \frac{J_0 z \eta}{V_t} \tag{3.20}$$

where J_0 is the exchange current density (A/cm^2).

The resistive term connected with charge transfer, called the charge transfer resistance (R_{ct}), is given by Equation (3.21). This defines an ion mobility in the system in relation to thermal voltage and exchange current density.

$$R_{ct} = \frac{V_t}{J_0 z} \tag{3.21}$$

For a highly mobile system ($J_0 \rightarrow \infty$), the R_{ct} value approaches zero. This is the condition where an electrode-electrolyte system is ideally non-polarisable. In this condition charge

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transfer occurs moving the system from its equilibrium. Whereas for a highly immobile system ($J_0 \rightarrow 0$) the R_{ct} value approaches infinity, thus the system will behave as an ideal capacitor (ideally polarized) with no charge transfer (Faradaic impedance is zero) process occurring.

In the case of an AC signal stimulating a metal electrode, the interfacial impedance will depend on the frequency. At higher stimulus frequency the ions (from the diffuse cloud) will still agglomerate near the OHP, however as the frequency increases it becomes more difficult for them to follow the AC signal, thus the influence of the diffuse ion cloud decreases. This frequency dependent behaviour is known as the Warburg (diffusional) impedance (Equation 3.22) [111, Chapter 10]. The Warburg impedance (Z_w) becomes significant at low frequencies where the ion species from the diffuse cloud can influence the Faradaic impedance of the interface. As the frequency increases the charge transfer resistance (kinetics) determines the net current density, where Z_w tends towards zero. R_w and C_w are the diffusion resistance and capacitance respectively.

$$Z_w = R_w + \frac{1}{j\omega C_w} \tag{3.22}$$

The same applies in a system with a slow electrochemical reaction, where J_0 is small thus R_{ct} dominates and is proportional to ω^{-1} (e.g. a protein adsorbed onto the metal electrode surface will limit the effective charge exchange area) [112]. On the other hand if the charge transfer reaction proceeds rapidly in the system, the net current is limited by the diffusion of reactants (J_0 is large). In this case the Warburg diffusion impedance dominates and the Faradaic impedance is proportional to $\omega^{-1/2}$.

As the metal electrode comes in contact with a liquid phase solution a current spreading from the electrode to a conductive medium is highly dependent on the interface geometry, thus the spreading resistance (R_s) can be defined. Since microelectrodes used in an electrophysiological measurements have complex geometries and surface roughness need to be taken into an account, the derivation for R_s for such electrodes becomes complex. In addition the complexity increases for electrodes with a modified surface, for example by depositing platinum-black. A sponge-like material, platinum-black effectively increases the surface area of the electrode [113]. Although the effective surface of the electrode can be decreased by protein adsorption as discussed above, for a planar disk [114] and rectangular [115] shape electrode the R_s is given by Equation 3.23 and 3.24 respectively. Where ρ_m is the resistivity of the electrolyte solution and r is the electrode radius.

$$R_s = \frac{\rho_m}{4r} \tag{3.23}$$

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$$R_s = \frac{\rho_m}{\pi l} \ln\left(\frac{4l}{w}\right) \tag{3.24}$$

l and w are the length and width of the electrode respectively.

The above defined parameters together represent components of an equivalent circuit model for the metal electrode-electrolyte interface shown in Figure 3.6.

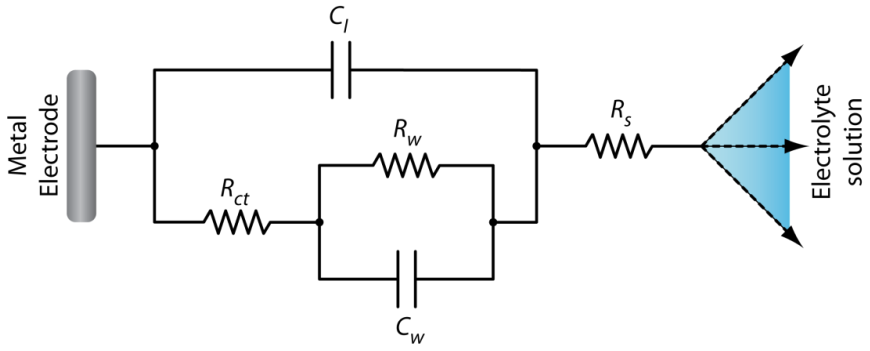

Figure 3.6: An equivalent circuit model of the metal electrode-electrolyte interface [111, Chapter 8].

The parasitic impedance components, as shown in Figure 3.6, influencing the metal electrode-electrolyte interface are frequency dependent thus the electrode should be stimulated at high frequencies (>> 1 kHz) where these components are negligible. Another solution is to use four terminal (Kelvin bridge) measurement methodology as shown in Figure 3.7. Current I supplied by low input impedance terminals (A_1 and A_2) is passed through the device-under-test (DUT) and is measured by an ammeter (A). The potential across the DUT is measured by a voltmeter (V) through the high input impedance terminals (V_1 and V_2). The registered potential is not influenced by parasitic impedances due to a no current being drawn by these electrodes (the relation between the electrode polarisation potential and the current is linear), thus the ratio of the registered potential and current through the DUT is a measure of its impedance independent of parasitic impedances. Therefore Kelvin bridge technique has been utilised together with a flow-through Coulter counter presented in further sections of this thesis.

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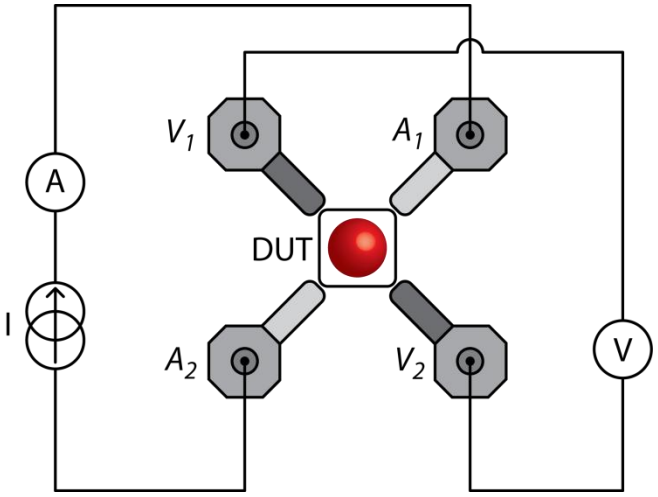

Figure 3.7: Four terminal measurement methodology.

3.3.2 Charge transfer across the interface

The kinetics of charge transfer across an interface between two distinct phases is given by the Butler-Volmer equation [111, Chapter 3]. The Equation 3.25 is not limited to describing the charge exchange process across a solid-liquid interface, but can also be applied to any active process where charge exchange takes place. It forms a basis for deriving the potential difference across an arbitrary interface separating two distinct phases.

$$J_p = z_p F \vec{k}_p \left[X_p\right]_\beta exp\left(\frac{z_p F \varsigma \Delta\phi}{RT}\right) - z_p F \overleftarrow{k}_p \left[X_p\right]_\alpha exp\left(\frac{-z_p F(1-\varsigma)\Delta\phi}{RT}\right) \quad (3.25)$$

The exchange net current density (J_p) is described in terms of the potential difference across the interface, $\Delta\phi = \left(\phi_\beta - \phi_\alpha\right)$ and the concentration of the ionic species p in the solid $[X_p]_\beta$ and liquid $[X_p]_\alpha$ phase. The components $\vec{k}_p$ and $\overleftarrow{k}_p$ are the heterogeneous rate constants for the forward and reverse ionic currents flowing through the interface. z_p is the formal charge of p and ς is the symmetry coefficient between the forward and reverse fluxes. z_p can range from 0 to 1 with a typical value of 0.5 [116]. T, F, and R are the absolute temperature, Faraday constant and universal gas constant respectively.

For the discrete interface between a solid (β-phase) and an electrolyte solution (α-phase), J_p due to a flow of a single ionic species p across the interface is described in general as a difference between ion fluxes out of the solid ($\vec{J}_p$) and into the solid phase ($\overleftarrow{J}_p$). The exchange net current density previously given by Equation 3.20, for the p^{th} ionic species, is given by [116].

$$J_p = \vec{J}_p - \overleftarrow{J}_p \quad (3.26)$$

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In a situation where various mobile ionic species are present in the system, the exchange currents for all of the *m* ionic species present must be summed to derive the total net current [116]:

$$J_{tot} = \sum_{p=1}^{m} \vec{J}_p = \sum_{p=1}^{m} \left(\vec{J}_p - \bar{J}_p \right) \tag{3.27}$$

At an interface with multiple net currents (corresponding to multiple ionic species) Equations 3.25 and 3.27 provide a complete description of the charge exchange and the potential difference between the two phases. All of the net exchange currents therefore are governed by a single interfacial potential that is the same for all ionic species. Furthermore ionic species having the largest exchange currents will dominate the total net current, thus the fastest exchanging ions will determine the interfacial potential. In most cases it can be approximated that the interfacial potential depends only on the dominant forward and reverse net exchange currents, which originate from the same or multiple ionic species present at the interface.

The $J/\Delta\phi$ curves that describe a situation where the forward and reverse net exchange currents are dominated by a single ionic species, thus defining the potential across the interface, are shown in Figure 3.8. For the total measured current (shown as a dashed line) $J_{tot}=0$ the value of $\Delta\phi$ is defined as an open circuit potential difference (OCP). It is also an equilibrium potential ($\Delta\phi_{p(eq)}$) where the forward and reverse currents densities for the single ionic species ($p=1$) are equal to each other $\left(\vec{J}_p = \bar{J}_p \right)$. Considering only a single ionic species ($J_{tot} = J_p$) and solving Equation 3.25 to derive the $\Delta\phi$, leads directly to an expression for the Nernst potential:

$$\Delta\phi = \frac{RT}{z_p F} \ln \frac{\bar{k}_p}{\bar{k}_p} + \frac{RT}{z_p F} \ln \frac{[X_p]_\alpha}{[X_p]_\beta} = \phi_k + \frac{RT}{z_p F} \ln \frac{[X_p]_\alpha}{[X_p]_\beta} \tag{3.28}$$

If the concentration of pth ions in the solid phase doesn't vary (it acts as a large buffer with ions) then the $[X_p]_\beta$ can be combined with the constant ϕ_k, to derive

$$\Delta\phi = \phi_k' + \frac{RT}{z_p F} \ln [X_p]_\alpha = \phi_k' + 2.303 \frac{RT}{z_p F} \log [X_p]_\alpha \tag{3.29}$$

The characteristics of $\Delta\phi$, as a function of $[X_p]_\alpha$, are linear with a curved slope of 59.2 mv/decade for univalent ions ($z_p=1$) at a temperature of 25 ^{o}C. This is an ideal interface response also referred to as the Nernstian response [111, Chapter 3]. In electrochemical measurements specific membranes of ion-selective electrodes (ISEs) are chosen to selectively transport a single ionic species across the interface with a desirable Nernstian response (or closely related).

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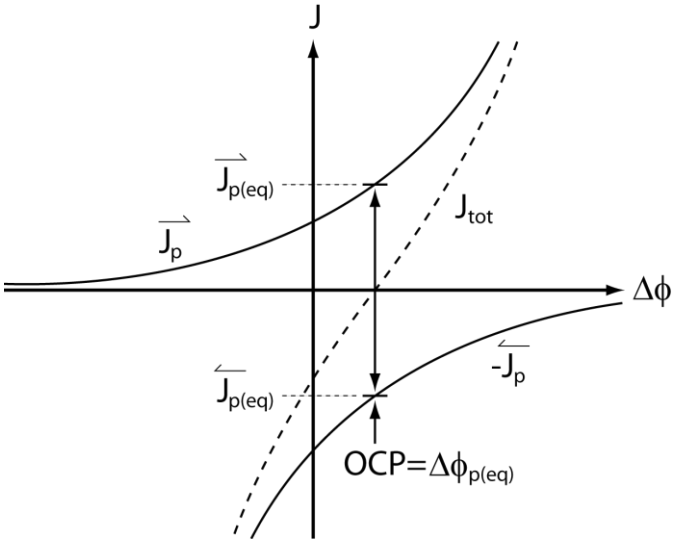

Figure 3.8: Graph of the forward and reverse ion-exchange currents dominated by a single ionic species in a function of an interface potential [116].

Consider a classical glass electrode [109] with a selective membrane used for the concentration measurement of the p^{th} ionic species in an electrolyte. The potential of the electrode is measured with respect to a reference electrode i.e. glass saturated calomel electrode (SCE). Thus the electrochemical cell is described as [117, Chapter 3]:

$$\underbrace{Hg \,||\, Hg_2Cl_2KCl(salt)}_{SCE} \,||\, Electrolyte \,||\, \underbrace{Glass\ membrane \,||\, \overbrace{HCl(0.1M)}^{Internal reference} \,||\, AgCl \,||\, Ag}_{Glass electrode}$$

where || represents a phase boundary where the interfacial potential difference is developed between the two distinct phases. The SCE creates an ohmic contact to the electrolyte solution (salt bridge) through a porous membrane. The potential difference is developed between the glass electrode with an ion permeable membrane and the analyte solution. If the membrane is selective towards the p^{th} ionic species the cell potential E is given by:

$$E = E_0 + \frac{RT}{z_p F}\ln[X_p]_{sol} = E_0 + 2.303\frac{RT}{z_p F}\log[X_p]_{sol} \tag{3.30}$$

where E_0 is the sum of the potential differences at all other interfaces including the ohmic contact between SCE and the electrolyte (standard electrode potential). E_0 is measured during a calibration procedure in a standard solution with a known ionic concentration $[X_p]_{sol}$. Measuring the specific ion transport amount through the selective membrane allows the determination of the concentration of that ionic species in the electrolyte solution. In 1909, Sørensen introduced the concept of pH, which is defined as the negative logarithm of the hydrogen protons (H^+) concentration (*pondus hydrogenii* – hydrogen exponent) in the analyte solution (Equation 3.31) [118, Chapter 71], thus the degree of acidity or basicity of the electrolyte.

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$$pH = -\log[H^+] \tag{3.31}$$

As the concept of pH measurement was studied more deeply it was recognized that it was in fact the measurement of hydrogen ion activity also referred to as the effective concentration (Equation 3.32).

$$pH = -\log a_{H^+} = -\log \gamma[H^+] \tag{3.32}$$

where: a_{H^+} is the hydrogen proton activity and γ is the activity coefficient.

Consider hydrogen ion concentration measurement using an ion selective electrode towards that ionic species. Substituting Equation 3.31 into 3.30 and using given values of R = 8.3144 J K^{-1} mol^{-1}, T = 298 K, z_{H^+}= 1 and F = 96485.3399 C mol^{-1} produces:

$$E = E_0 - 2.303\frac{RT}{z_p F}\log[H^+] = E_0 - 0.05916V \cdot pH \tag{3.33}$$

From Equation (3.33) it can be seen that for the electrolyte ionic concentration change the cell potential will vary with a rate of 59.16 mV/pH which is known as a Nernstian response for the hydrogen ion measurement.

3.3.3 Electrolyte-insulator-semiconductor interface

The interface between the insulator and the electrolyte consists of three distinct layers with distributed charge species shown in Figure 3.9. The composition and locus of these layers have been introduced in Section 3.3.1. When in contact with the electrolyte, the insulator's surface hydrolyses forming surface groups. These groups can have several charge states: positive, negative or neutral, depending on the ionic concentration (pH while considering hydrogen ions) of the electrolyte solution. A solid surface will carry zero charge while exposed to the electrolyte with a specific pH index which defines the pH of the point of zero charge specific to that surface "pH(pzc)" [119].

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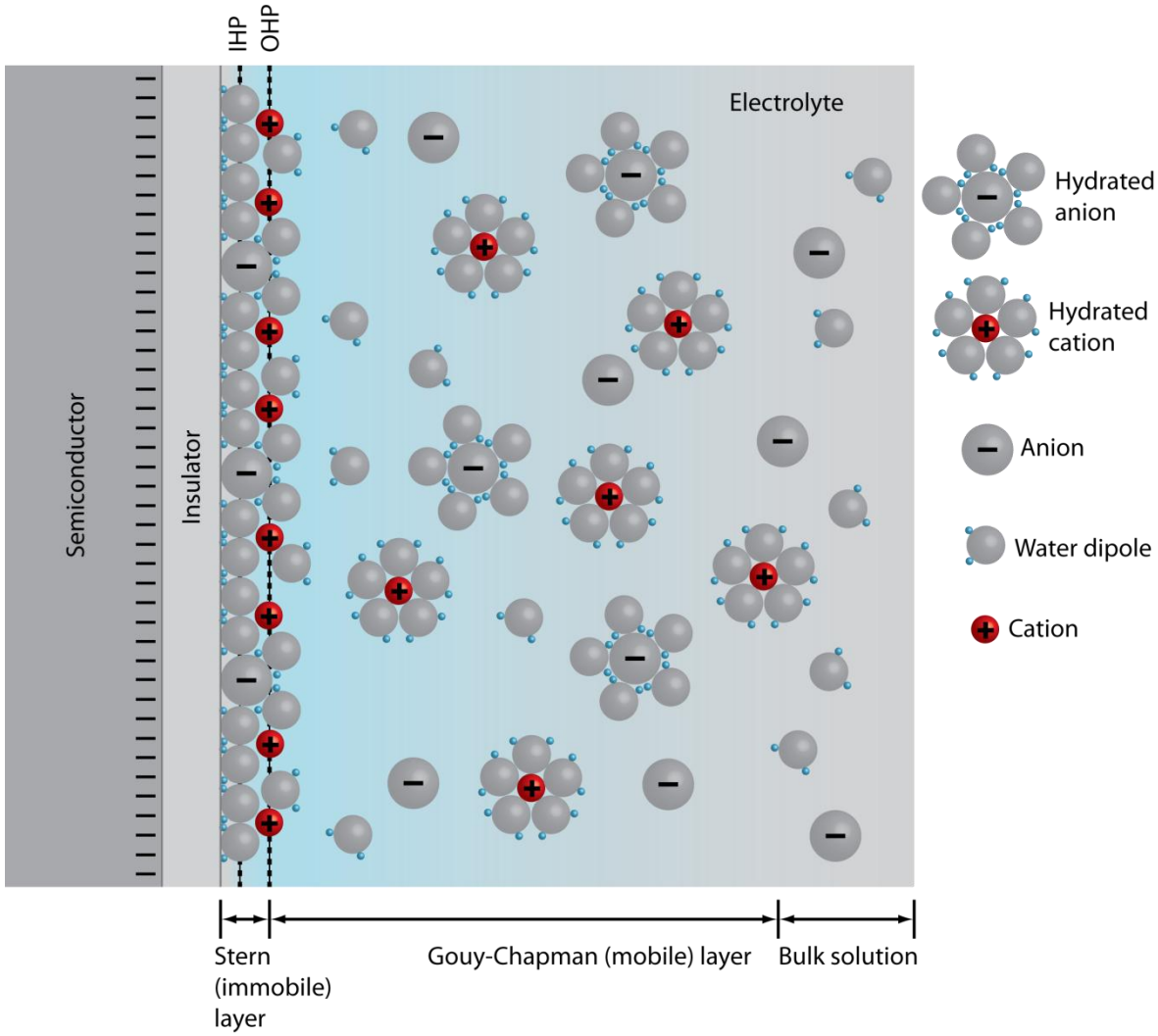

Figure 3.9: Electrolyte-insulator-semiconductor (EIS) interface [109].

Both positive (H^+) and negative (OH^-) ions are responsible for the insulator's surface charge state, thus they are called potential-determining ions. Therefore, the charge distribution and potential gradient in the EIS interface depends on whether the surface adsorbs the negative charge (Figure 3.10 (a)) or the positive charge (Figure 3.10 (b)).

The total charge density in the OHP due to non-specific ion adsorption is σ_O and excess charge density in the diffuse plane is σ_D so that the total charge in the electrolyte is $\sigma_O + \sigma_D$. In the solid phase the total charge density in the semiconductor region is σ_S thus applying the concept of charge neutrality:

$$\sigma_D + \sigma_O + \sigma_S = 0 \tag{3.34}$$

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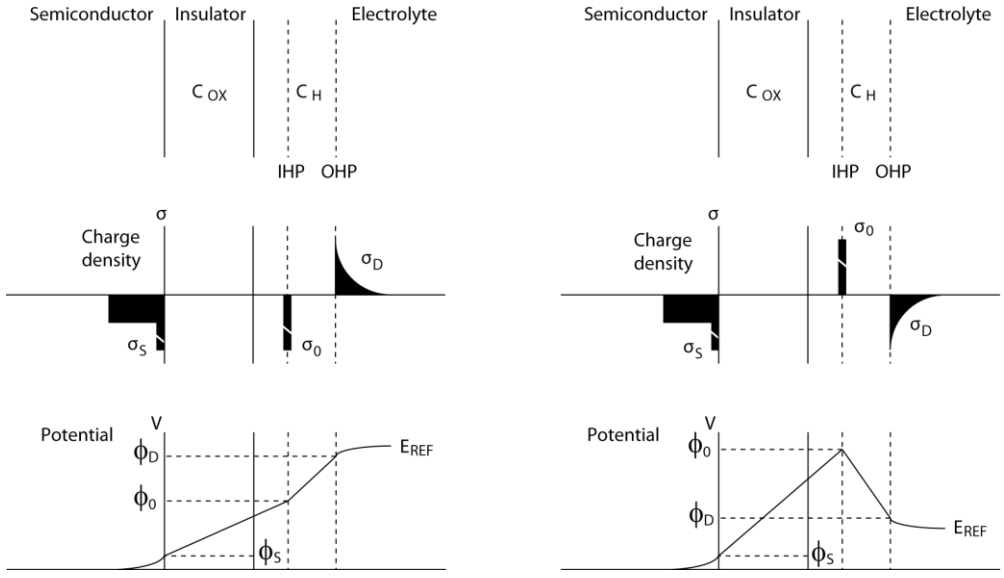

(a) pH > pH(pzc) **(b) pH < pH(pzc)**

Figure 3.10: Graphs of the charge and potentials distribution in the EIS system [119].

Furthermore if the semiconductor bulk potential is set to zero and the electrolyte bulk potential is set to E_{REF} then, since the potential across the EIS interface must be continuous:

$$E_{REF} + \left(\phi_D - E_{ref}\right) + \left(\phi_O - \phi_D\right) + \left(\phi_S - \phi_O\right) - \phi_O = 0 \tag{3.35}$$

and,

$$\phi_O - \phi_S = -\frac{\sigma_S}{C_{OX}} \tag{3.36}$$

$$\phi_O - \phi_D = -\frac{\sigma_D}{C_H} \tag{3.37}$$

$$\phi_D - E_{REF} = -\frac{2kT}{q}\sinh^{-1}\left(\frac{\sigma_D}{\sqrt{8\varepsilon_r kTc}}\right) \tag{3.38}$$

where: k is the Boltzmann's constant, ε_r is the electrolyte permittivity, and c is the ionic concentration in the electrolyte. The Equation (3.38) is the Gouy-Chapman model for the diffuse layer [111, Chapter 13]. Combining (3.35) and (3.38) produces:

$$E_{REF} + \underbrace{\left[-\frac{2kT}{q}\sinh^{-1}\left(\frac{\sigma_D}{\sqrt{8\varepsilon_r kTc}}\right) - \frac{\sigma_D}{C_H}\right]}_{\phi_{EI} = -\Delta\phi} + \underbrace{\left[\frac{\sigma_S}{C_{OX}} - \phi_S\right]}_{\phi_{IS}} = 0 \tag{3.39}$$

where: E_{REF} the electrolyte potential applied through the reference electrode, ϕ_{EI} and ϕ_{IS} are the potentials at the electrolyte-insulator and at the insulator-semiconductor interface respectively. Equation (3.39) gives the relationship between the interface potential difference $\Delta\phi$ and the charge density across the EIS system.

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The above description explains the interaction in an EIS system where ions are mobile in an immobile bulk solution however if an electrolyte flows (induced by electrostatic or mechanical means) along a charged surface, the ionic species located in the IHP and OHP will stay adsorbed to the charged surface creating a thin layer of immobile fluid known as a hydrodynamically stagnant layer. This layer extends from the solid surface to a distance d_{ek} (Figure 3.11), where a hydrodynamic plane of shear is located [120]. Consider the two cases: some distance $x < d_{ek}$ in respect to the wall where no hydrodynamic flow can occur and $x > d_{ek}$ where hydrodynamic flow occurs, will have different viscosities thus it can be said that viscosity is distance dependent. For $x > d_{ek}$ the hydrodynamically mobile layer carries charge in which the electrokinetic charge density σ_{ek} can be defined. The plane of shear is the sharp boundary between the two, hydrodynamically immobile and hydrodynamically mobile layer. The potential which occurs at that plane with respect to the charged solid surface is identified as the electrokinetic or zeta-potential (ζ) [120] (Figure 3.11). Mathematically the ζ is given by Equation (3.40) [121, Chapter 6]. In practice it can be said that, ζ-potential is equal or lower in magnitude than the potential at the diffuse plane (ϕ_D).

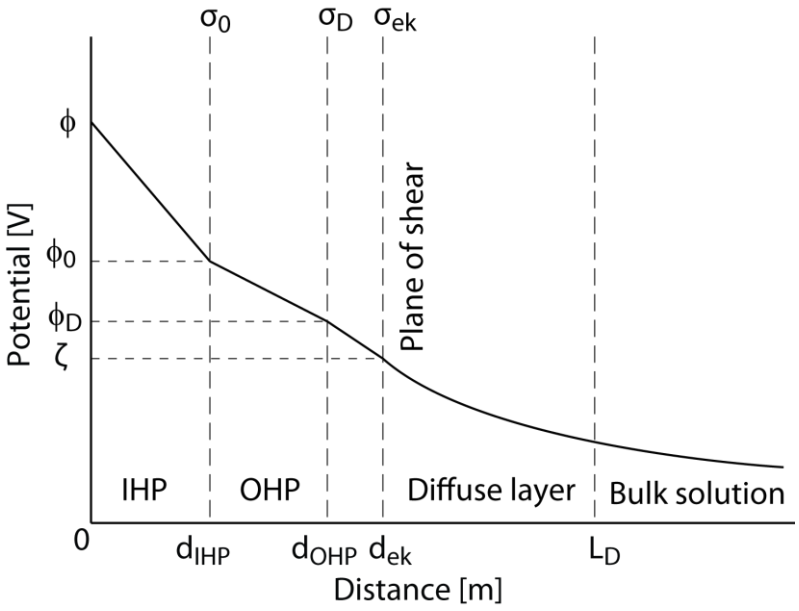

Figure 3.11: Potentials and charge distribution in the EIS system [120].

Furthermore the difference between the ϕ_D and ζ is a function of ionic strength in the electrolyte solution. At a low ionic strength the decay of the interface potential difference as a function of distance from the charged solid surface is small thus $\zeta \cong \phi_D$. At the high ionic strength, the decay is steeper and $|\zeta| \leq |\phi_D|$.

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$$\zeta = -\frac{\mu_{EO}\theta}{\varepsilon_r} \tag{3.40}$$

where: μ_{EO} is the electro-osmotic mobility and θ and ε_r are the electrolyte absolute viscosity and permittivity respectively.

The relationship between the ζ-potential and the pH index of the electrolyte solution is shown in Figure 3.12. The pH at which the ζ-potential is zero is defined as the isoelectric point (IEP).

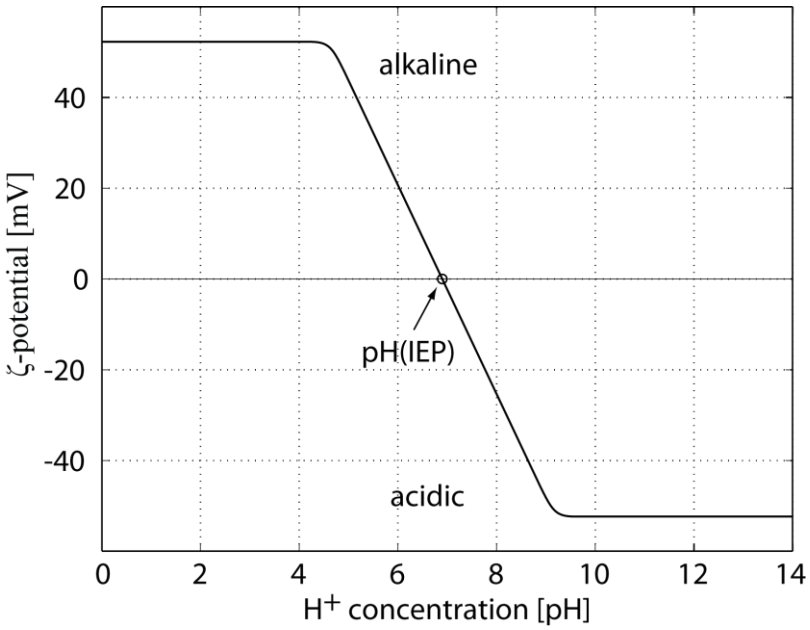

Figure 3.12: General dependence between ζ-potential and pH showing dissociation and adsorption of the acidic or alkaline surface groups [122].

3.3.4 Site binding model

For an ideally unblocked interface (R_{ct} is zero) separating an electrolyte and an insulator phase various ionic species can exchange freely between the two. The interface with a low R_{ct} for a specific ionic species can be realised in an EIS system if the insulator is doped with impurity atoms that can perform the ion exchange. Considering a glass electrode, a glass membrane can be doped with lithium atoms to facilitate ion exchange currents with the hydrogen cations in the solution [123, Chapter 3]. At the opposite extreme is an ideally blocked also referred as an ideally polarised interface (R_{ct} is infinite). Where charges are present at the interface however no ion exchange takes place between the two phases. The charge distribution and the potential gradient in such an EIS system is dominated only by electrostatic forces. Furthermore, since the insulator surface has no specificity towards certain ionic species adsorption, the interface's electrochemical response is dominated by the

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total ionic strength of the electrolyte solution. In this case the insulator surface exhibits no ion exchange with the electrolyte but nor is it completely inert. The site-binding model developed by Yates *et. al.* describes the interaction at a general oxide-electrolyte interface [124]. It was later adopted to the electrolyte-SiO_2-Si system developed by Siu and Cobbold [119] and Bousse *et. al.* [125].

Considering a SiO_2 surface when exposed to an electrolyte solution, it hydrolyses forming surface silanol (*SiOH*) groups (Figure 3.13). These groups are amphoteric, meaning that they are capable of adsorption of positive or negative charges thus the surface can be charged positively, negatively or be neutral depending on the pH of the aqueous solution. The acidic and basic character of the neutral site *SiOH* is defined by the succeeding reactions and dissociation constants[20] K_{A1} and K_{A2} [126, 127]:

$$SiOH_2^+ \leftrightharpoons SiOH + H^+ \qquad K_{A1} = \frac{[SiOH][H^+]_S}{[SiOH_2^+]} \tag{3.41}$$

$$SiOH \leftrightharpoons SiO^- + H^+ \qquad K_{A2} = \frac{[SiO^-][H^+]_S}{[SiOH]} \tag{3.42}$$

where: the index *S* indicates a surface quantity. The density of active groups on the surface N_{A1} and the charge density per unit area σ_{0_A} are given by:

$$N_A = [SiOH_2^+] + [SiOH] + [SiO^-] \tag{3.43}$$

$$\sigma_{0_A} = q([SiOH_2^+]) - [SiO^-] \tag{3.44}$$

[20] The dissociation constant is a type of equilibrium constant that measures the tendency of the larger object to dissociate reversibly from the smaller object.

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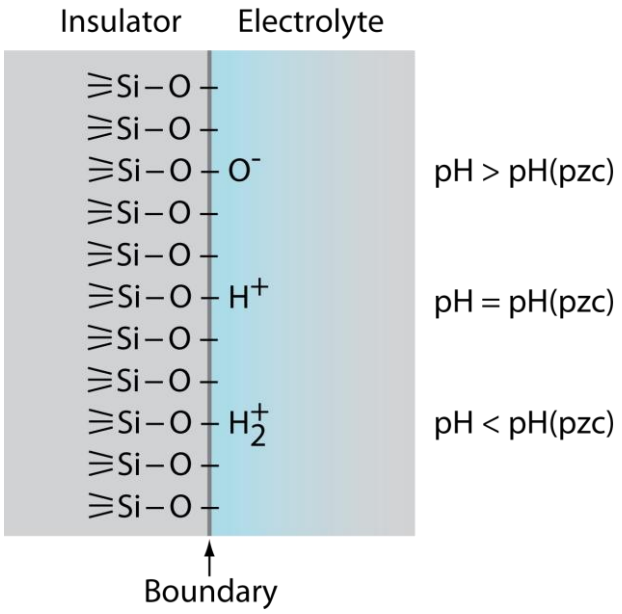

Figure 3.13: Surface groups and reactions for silicon dioxide [119].

Due to a temperature influence (thermal mixing), the concentration of H^+ cations on the insulator's surface can be related to the bulk H^+ cations concentration which is given by Boltzmann statistics [124]:

$$[H^+]_S = [H^+]\exp\left(-\frac{q\Delta\phi}{kT}\right) \tag{3.45}$$

Multiplying Equations (3.41) and (3.42) and replacing for $[H^+]_S$ in Equation (3.45) produces:

$$[H^+] = \sqrt{K_{A1}K_{A2}}\exp\left(\frac{q\Delta\phi}{kT}\right)\sqrt{\frac{[SiOH_2^+]}{[SiO^-]}} \tag{3.46}$$

For $\Delta\phi = 0$ and $\sigma_{0_A} = 0$ (i.e.$[SiOH_2^+] = [SiO^-]$) from (3.46) is can be seen that $[H^+] = \sqrt{K_{A1}K_{A2}}$. It gives the required hydrogen cations concentration in the electrolyte to develop an electrically neutral insulator surface which is also referred as pzc for that surface. The pH index at pzc is marked $pH(pzc)_A$ and can be combined into (3.46) to produce:

$$2.303\left(pH\left(pzc\right)_A - pH\right) = \left(\frac{q\Delta\phi}{kT}\right) + \ln F_A \tag{3.47}$$

The above equation links an interface charge, potential and an electrolyte pH while the function:

$$F_A = \sqrt{[SiOH_2^+]/[SiO^-]} \tag{3.48}$$

plays a key role in an electrochemical response of the insulator's surface. To solve this function, the normalised net charge on the surface is defined as:

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$$\chi_A = \frac{\sigma_{0A}}{qN_A} = \frac{[SiOH_2^+] - [SiO^-]}{[SiOH_2^+] + [SiOH] + [SiO^-]} \tag{3.49}$$

To find χ_A as a function of F_A the (3.49) is divided through by $[SiO^-]$:

$$\chi_A = \frac{F_A^2 - 1}{F_A^2 + F_A\sqrt{K_{A1}/K_{A2} + 1}} \tag{3.50}$$

Equation (3.50) can be inverted by introducing $\delta = 2\sqrt{K_{A2}/K_{A1}}$ and selecting the positive root of the quadratic to produce: $F_A(\chi_A)$:

$$F_A^2(\chi_A - 1) + F_A\frac{2\chi_A}{\delta} + \chi_A + 1 = 0 \tag{3.51}$$

$$F_A = \frac{(\chi_A/\delta) + \sqrt{(\chi_A/\delta)^2(1-\delta)^2 + 1}}{1 - \chi_A} \tag{3.52}$$

Equation (3.47) gives the electrolyte pH as a function of both $\Delta\phi$ and σ_{0A}, and a relationship between $\Delta\phi$ and σ_{0_A}(3.53) is found using the definition of $\Delta\phi$ expressed by (3.39).

$$\Delta\phi = \frac{2kT}{q}\sinh^{-1}\left(\frac{\sigma_D}{\sqrt{8\varepsilon 2kTc}}\right) + \frac{\sigma_D}{C_H} \tag{3.53}$$

Applying the charge neutrality concept in the EIS structure (Figure 3.9) produces:

$$\sigma_D + \sigma_{0A} = \Delta\sigma_S = -\sigma_S \tag{3.54}$$

Assuming that $\Delta\sigma_S = 0$ thus $\Delta\sigma_S = -\sigma_{0_A}$ [125], it is now possible to solve for $\Delta\phi/pH$ utilising a parametric method. Taking χ_A as a parameter, the $\Delta\phi$ is derived from (3.53), and F_A is found with (3.52). These two are then combined into (3.47) to derive the electrolyte solution pH index. By using values of the equilibrium constants and the surface site densities for the SiO_2 : $K_{A1} = 10^{1.8}$, $K_{A2} = 10^{-6.2}$ and $N_A = 5 \times 10^{18}$ sites/m^2 [126] with the site binding model it can be shown that the SiO_2 surface has a low electrochemical (sub Nernstian) response of -46.3 mV/pH (at an electrolyte pH 6). For this particular surface the point of zero charge occurs at an electrolyte pH 2.2, thus nonlinearity in the electrochemical response can be seen for the acidic pH range (Figure 3.14) [128]. The nonlinearity in the SiO_2 response to the electrolyte pH variation has been experimentally confirmed, where different pH sensitivities are measured in the low (acidic) and high (alkali) pH electrolytes (Section 2.5). A SiO_2 based pH sensitive surface has its limitations as described above however these values will vary with insulator composition and its deposition method i.e. chemical vapour deposition (CVD) or thermal oxide. This shows that an alternative insulator material, expressing high linear electrochemical response is desired [126].

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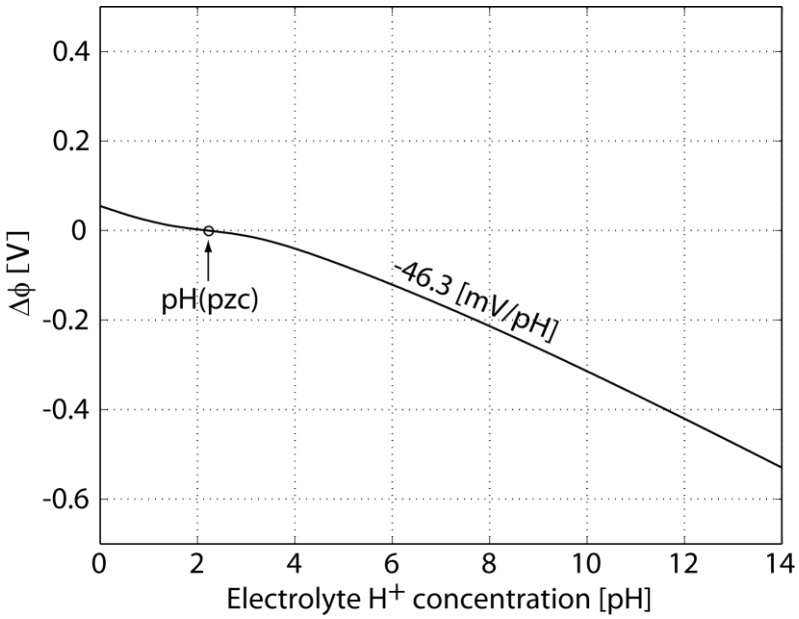

Figure 3.14: Theoretical electrochemical response of a SiO_2 surface.

Silicon nitride (Si_3N_4) has superior properties over SiO_2 thus has been used as a replacement for SiO_2 in an electrochemical measurement. It is assumed that on the Si_3N_4 surface, each of the nitrogen atoms bonds to three silicon atom, hereby forming Si_3N sites. While the surface is placed in contact with an aqueous electrolyte, these sites take part in a hydrolysis reaction [126]:

$$Si_3N + H_2O \rightarrow Si_2NH + SiOH \tag{3.55}$$

The *Si_2NH* site may be further hydrolysed to produce:

$$Si_2NH + H_2O \rightarrow SiNH_2 + SiOH \tag{3.56}$$

whereby a complete hydrolysis reaction leads to both *SiOH* – amphoteric (index *A*) and *$SiNH_2$* – basic (index *B*) surface groups as shown in Figure 3.15. Measurements carried out by Matsuo and Esashi using Auger electron spectroscopy showed an excess of oxygen in the first few atomic layers thus an oxidised surface after 14h in water [80]. The *SiOH* sites express behaviour according to (3.41) and (3.42), while the *$SiNH_2$* sites react according to:

$$SiOH_3^+ \leftrightharpoons SiNH_2 + H^+ \qquad K_B = \frac{[SiNH_2][H^+]_S}{[SiNH_3^+]} \tag{3.57}$$

Considering only the *$SiNH_2$* sites, their surface density N_B and the charge per surface unit area σ_{0_B} are:

$$N_B = [SiNH_2] + [SiNH_3^+] \tag{3.58}$$

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$$\sigma_{0B} = q[SiNH_3^+] \tag{3.59}$$

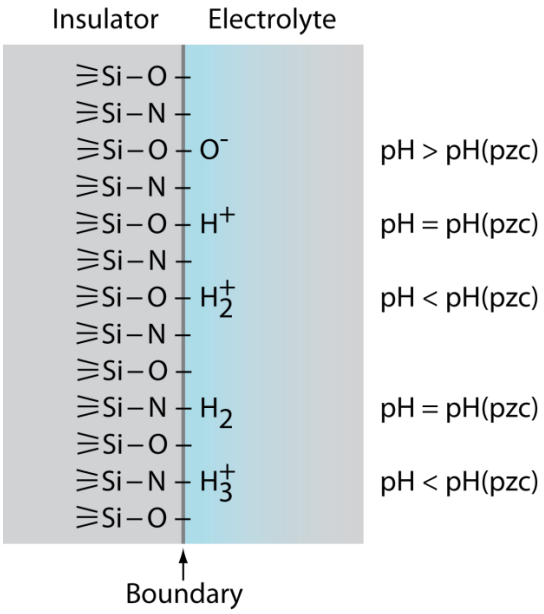

Figure 3.15: Surface groups and reactions for silicon nitride.

Applying the Boltzmann distribution as above produces:

$$2.303\left(pK_B - pH\right) = \frac{q\Delta\phi}{kT} + \ln\left(\frac{[SiNH_3^+]}{N_B - [SiNH_3^+]}\right) \tag{3.60}$$

where: pK_B = -*log* K_B. This system has the positive and the neutral sites thus a point of zero charge occurs when $[SiNH_3^+]$ has zero value. Comparing Equations (3.60) and (3.47) shows that an equivalent *F*-function for the *SiNH₂* sites is given by:

$$F_B = \frac{[SiNH_3^+]}{N_B - [SiNH_3^+]} = \frac{\chi_B}{1 - \chi_B} \tag{3.61}$$

In consequence, now considering both sites, the *SiOH* and *SiNH₂*, the total density of surface groups for the Si_3N_4 is given by:

$$N = N_A + N_B \tag{3.62}$$

and,

$$\frac{N_A}{N} + \frac{N_B}{N} = f_A + f_B = 1 \tag{3.63}$$

Therefore the complete normalised charge per surface unit area χ is given by:

$$\chi = \frac{q\left([SiNH_2^+] - [SiO^-] + [SiNH_3^+]\right)}{N} = f_A\chi_A + f_B\chi_B \tag{3.64}$$

Applying previous definitions of χ_A and χ_B the χ is:

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$$\chi = f_A \frac{F_A^2 - 1}{F_A^2 + F_A\sqrt{K_{A1}/K_{A2}} + 1} + f_B \frac{F_B}{F_B + 1} \tag{3.65}$$

Subtracting (3.47) from (3.60) produces the ratio R between the functions F_A and F_B:

$$R = \frac{F_B}{F_A} = 10^{\left(pK_B - pH_{A(pzc)}\right)} = \frac{\sqrt{K_{A1}/K_{A2}}}{K_B} \tag{3.66}$$

The point of zero charge for the Si_3N_4 surface (with amphoteric and basic groups) occurs for $\chi=0$ and the electrolyte pH index equals pH(pzc). Adding the constant $2.303(pH(pzc) - pH(pzc)_A)$ to Equation (3.47) produces:

$$2.303\left(pH\left(pzc\right) - pH\right) = \frac{q\Delta\phi}{kT} + \ln F \tag{3.67}$$

Thus the new F-function is given by:

$$F = 10^{\left(pH(pzc) - pH(pzc)_A\right)} F_A \tag{3.68}$$

At the point of zero charge for the Si_3N_4 surface, $pH = pH(pzc)$ and $\Delta\phi = 0$, thus from (3.67), $F(pzc) = 1$. Combining $F(pzc) = 1$ into (3.68) gives $pH(pzc)$ described by:

$$pH\left(pzc\right) = pH\left(pzc\right)_A - \log F_A(pzc) \tag{3.69}$$

As for the SiO_2 surface with a single amphoteric site, the Si_3N_4 surface response (with the two amphoteric and basic sites) can be derived solving the Equation (3.67) for $\Delta\phi/pH$ utilising the parametric method [126]. To derive the response the following steps are performed:

1. define parameter χ_A;
2. evaluate F_A with (3.52);
3. derive F_B using (3.66);
4. calculate χ_B with (3.61);
5. calculate χ from (3.64);
6. find $\Delta\phi$ with (3.53);
7. calculate F using (3.68);
8. solve (3.67) to find the electrolyte pH index.

Values of the equilibrium constants and surface site densities for the Si_3N_4 surface are as follows: $K_{A1} = 10^{1.8}$, $K_{A2} = 10^{-6.2}$, $K_B = 10^{-10}$, $N_A = 3 \times 10^{18}$ sites/m^2, and $N_B = 2 \times 10^{18}$ sites/m^2 [126]. Following the above procedure and a given set of parameters values it can be said that the Si_3N_4 surface has a theoretical electrochemical response of -56.7 mV/pH with the point of zero charge located at an electrolyte pH index of 6.5 (Figure 3.16). Fur-

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thermore, the Si_3N_4 response is linear, which is due to the $SiNH_2$ surface groups. The response linearization occurs due the two types of sites being able to exchange their charge. If the basic sites are positively charged they will repel cations from the surface thus alter amphoteric sites to become negatively charged. As result the surface sites are constantly charged leading to a near Nernstian surface response [126].

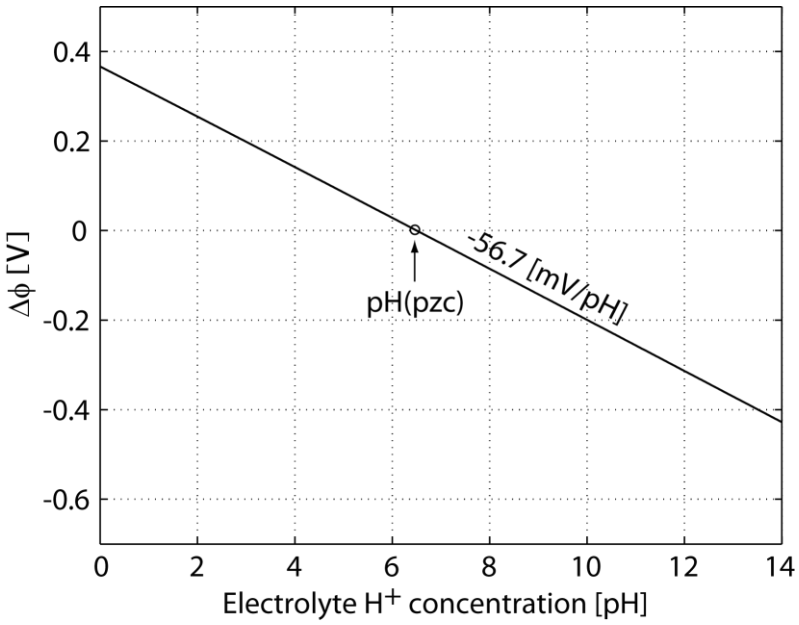

Figure 3.16: Theoretical electrochemical response of a Si_3N_4 surface.

3.4 The Ion Sensitive Field Effect Transistor

The glass-electrode based electrochemical sensor is unsuitable for a high scale of integration. A high scale of integration with low power operation became possible with the introduction of the ISFET concept in the early seventies of 20th century [78]. The operation of an ISFET is best explained by making an analogy to the MOSFET operating principle. Consider an n-channel MOSFET, where a positive voltage is applied to a highly-doped polysilicon gate[21] terminal which attracts electrons from the p-type silicon substrate to the surface below the gate oxide (Figure 3.17 (a)). When the gate voltage exceeds the threshold value an inversion region is created with a local change from p-type to an n-type material. Therefore, an n-type channel exists between the source and drain, thus allowing mobile electrons to flow between the two. To achieve this, the insulator surface potential – negative ($\phi_S = \phi_F$) in the initial condition must change to a positive value ($\phi_S = -\phi_F$), where ϕ_F is the Fermi potential. The minimum value of gate voltage required to produce

[21] Early MOSFETs had metal gates – hereof its name, later replaced by doped polysilicon, in contemporary technology metal gates return replacing polysilicon.

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this condition termed “strong” inversion is defined as the threshold voltage [69, Chapter 6] and is given by:

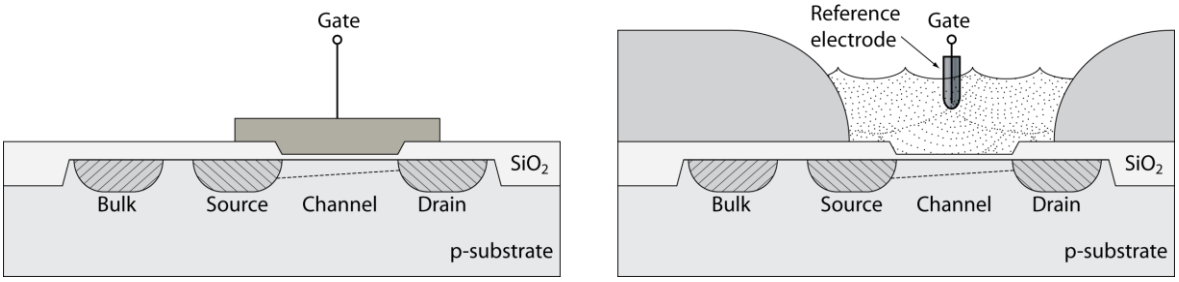
$$V_T = V_{FB} - \frac{Q_B}{C_{INS}} + 2\phi_F \tag{3.70}$$

where: V_{FB} is the flatband voltage, Q_B is the depletion charge in the silicon substrate, and C_{INS} is the capacitance of the gate oxide. The V_{FB} is defined by:

$$V_{FB} = \frac{\Phi_M - \Phi_S}{q} - \frac{Q_{SD} + Q_{INS}}{C_{INS}} \tag{3.71}$$

where: $(\Phi_M - \Phi_S)$ is the work function difference between the metal (or polysilicon) gate and the silicon substrate, q is the electron charge, Q_{SD} is the silicon surface charge density, and Q_{INS} is the total fixed oxide charge. As it can be seen from (3.70) and (3.71) the threshold voltage of the MOSFET is set by the work function of the interface materials and the charge accumulated between these two.

Consider an ISFET cross-section shown in Figure 3.17 (b); the metal (or polysilicon) gate of the MOSFET is replaced by a reference electrode-electrolyte-silicon dioxide system. Thus a metal reference electrode[22] makes an ohmic contact to the surface of the SiO_2 (insulator) through the electrolyte solution. Therefore provides a gate potential. As described in Section 3.3.3 the SiO_2 surface has amphoteric sites capable of adsorption/desorption of charged species thus charging/discharging the surface. This unique feature will influence the threshold voltage of the ISFET thus making it sensitive to the ionic composition in the electrolyte solution [78, 79, 95].



(a) MOSFET **(b) ISFET**

Figure 3.17: Cross-section of the MOSFET and the ISFET physical structure (diffusion contacts are avoided for clarity).

The Equation (3.72) describing the flatband voltage of the ISFET takes into account the potential at the gate oxide-electrolyte interface ($\Delta\phi + \chi_{ELEC}$) which is defined by the surface

[22] For the sake of simplicity a complex structure of the reference electrode is approximated to a single metal plate.

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dipole potential of the electrolyte χ_{ELEC} (it is a constant) and the ionic concentration dependent interface potential $\Delta\phi$ (set by EIS operation as explained in Section 3.3.4). The term E_{REF} is the reference electrode potential, where the associated work function Φ_M is included.

$$V_{FB} = E_{REF} - \Delta\phi + \chi_{ELEC} - \frac{\Phi_S}{q} - \frac{Q_{SD} + Q_{INS}}{C_{INS}} \tag{3.72}$$

The only term in (3.72) that changes with the ionic concentration is $\Delta\phi$, therefore measuring the electrolyte pH is a matter of measuring V_T (Equation 3.70). The ISFET is used as a transducer to measure ionic concentration, and with its high input impedance and a low output impedance it is suitable for that operation. However the ISFET sensing surface was found to have a sub-Nernstian or nonlinear response due to undesirable electrochemical reactions in the EIS system as previously discussed. What is more it uses the MOSFET fabrication process, allowing it to be integrated with front-end readout and signal processing circuitry on the same silicon substrate [129].

3.5 Coulter Counter

The first cytometer measuring electrical properties of a single cell developed by Coulter [37] used a single sensing aperture (electrical sensing zone). As the cell passes through the micro-channel it modulates the impedance measured between the two electrodes shown in Figure 3.18. This change is measured in terms of current or voltage (or both) alteration across the aperture (see Section 2.3).

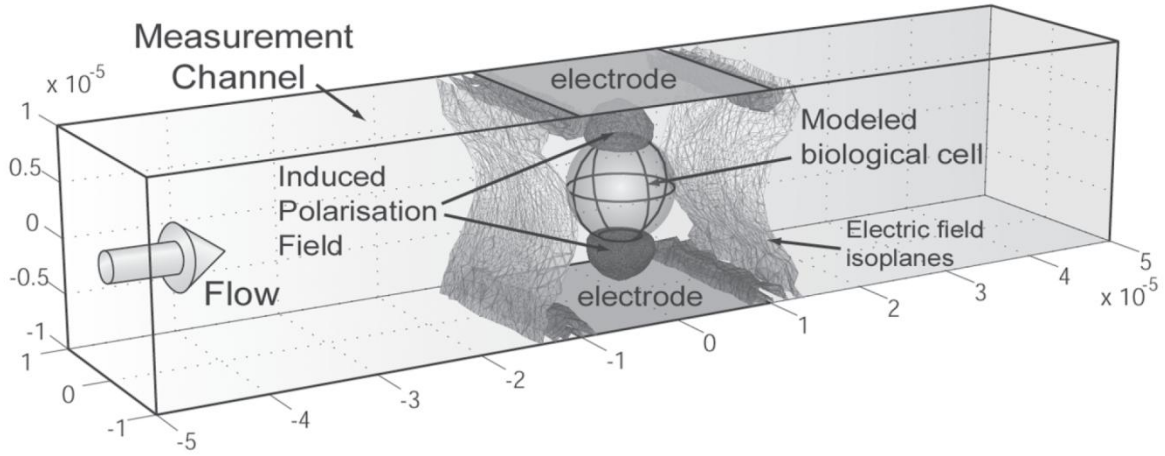

Figure 3.18: Graph of a cell positioned between two microelectrodes in a microfluidic channel [130].

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At frequencies where the total aperture impedance Z_{CH} is dominated by its resistance R_{CH} the relation between the particle size and the relative change in channel resistance ΔR_{CH} is given by [38, 41]:

$$\left|\frac{\Delta Z_{CH}}{Z_{CH}}\right| \approx \left|\frac{\Delta R_{CH}}{R_{CH}}\right| = \frac{d^3}{LD^2}\left[\frac{D^3}{2L^2} + \frac{1}{\sqrt{1+\left(\frac{D}{L}\right)^2}}\right] F\left(\frac{d^3}{D^3}\right) \tag{3.73}$$

where: d is the diameter of the cell, D and L are the channel diameter and length respectively, $F(d^3/D^3)$ is the correction factor that accounts for the current density variation within the aperture. Thus, rearranging (3.73) to produce the cell diameter gives:

$$d = \left[\left(\left|\frac{\Delta R_{CH}}{R_{CH}}\right| LD^2\right) \div \left(\frac{D^3}{2L^2} + \frac{1}{\sqrt{1+\left(\frac{D}{L}\right)^2}} F\left(\frac{d^3}{D^3}\right)\right)\right]^{\frac{1}{3}} \tag{3.74}$$

The Coulter counter operating at low frequency is limited by providing only the particle size information. Therefore measuring impedance of the cell at higher frequencies [131, 132] gives a broader spectrum of parameters. The AC Coulter counter measures dielectric properties (permittivity and conductivity) of the cell (membrane and plasma) as well as the suspension medium [100]. Measuring impedance at multiple frequencies enables the measurement of the membrane capacitance and the cytoplasm conductivity [56] and therefore observe the cellular mechanisms and the cell differentiation without a need for markers or any prior cell treatment [57]. Various cytometry-enabled sensor architectures have been developed (Table 3.1), however the most promising in terms of analyte sensing in a parallel fashion – thus increasing throughput and capability of integration in a multiple-sensor systems, are expressed by a flow-through approaches. Consider an impedance sensor where the sensing electrodes are embedded into the sidewalls of a sensing aperture shown in Figure 3.19. The principle of operation remains as for the classical Coulter counter however the analyte flows perpendicular to the sense electrode layout [8]. This arrangement allows embedding of a large number of apertures on a small area (Figure 3.19 (b)) thus it enables the flow-through methodology to be implemented in a CMOS-MEMS technology. Impedance is not the only electrical parameter of the cell that can be measured. The living cell's surface charge (ionic composition) varies according to the cell activity [133]. Therefore cell behaviour can be observed by measuring a membrane surface charge.

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The ISFET based ion sensor (see Section 3.4) has a capability of both measuring ionic composition and to be embedded in a flow-through sensing platform [9].

Architecture	No. of channels	Analyte	Measurement method	Ref.
Flow-through	1	45.6, 367, 867 µm polystyrene particles	Impedance, 50 kHz	[8]
Lateral	8	13 – 20 µm Juniperus scopulorum polen	Impedance, 60 kHz	[134]
Lateral	1	5 – 8 µm Human erythrocytes	Impedance, 1.7 and 15 kHz	[59]
Lateral	1	25 µm Polymer particles	Impedance, 50 kHz	[61]
Coplanar	1	5 – 8 µm Human erythrocytes	Impedance, 1 – 500 kHz	[101]
Coplanar	4	20 and 40 µm Polymer particles	Resistance, DC	[54]
Flow-through	1	ssDNA and dsDNA	Resistance, DC	[46]
Flow-through	1	dsDNA	Resistance, DC	[52]

Table 3.1: Single cell impedance microfluidic cytometry architectures.

The ionic concentration in the aperture will depend on the electrolyte composition i.e. the presence of the cell. The flow-through ion sensor measures a change in charged species concentration while the analyte passes through, where the number of distinct changes defines the number of flown cells. Therefore the flow-through ISFET sensor can be considered as a charge measuring Coulter counter. Furthermore both sensors, the Coulter counter and the flow-through ISFET, are compatible with a CMOS technology thus can be integrated on the same silicon dice together with readout electronics [135].

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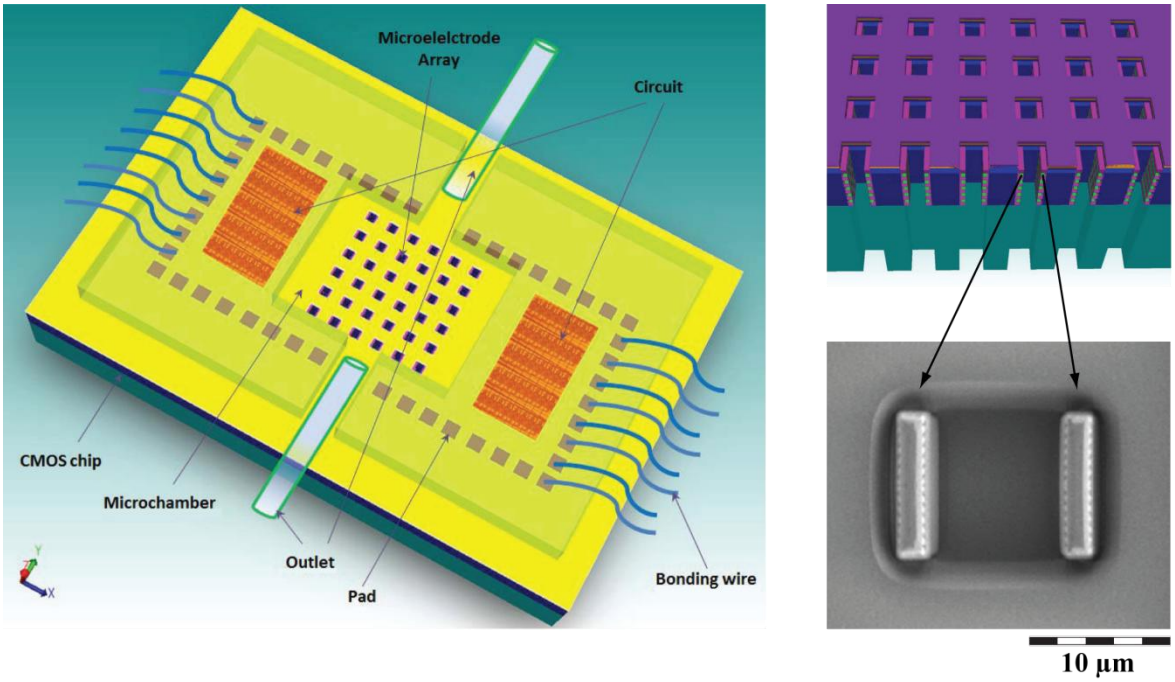

Figure 3.19: CMOS chip with embedded Coulter counters array. (a) Isometric projection, (b) Membrane cross-section and a top view of a single sensing aperture [135].

The device depicted in Figure 3.19 was fabricated in a standard CMOS technology and in-house post-processed using DRIE to open the sensing apertures. However as can be seen in Figure 3.19 (b) a micro-pore was over etched exposing the metal electrodes pair (which according to the device concept should to be encapsulated in an inter-layer dielectric – SiO_2). Furthermore no measurement results were published except the theoretical simulation. The device presented in this work uses the similar CMOS compatible DRIE postprocessing technique where the on chip membrane was developed according to the specification leading to successful measurement results presented in the experimental section of this thesis.

The concept of the Coulter counter evolved not only towards a parallelization of a measurement process [134] but nanometre size molecules sensing also became possible. Integrating high throughput with a small molecule sensing capability in sophisticated nanopore devices [136] for single stranded DNA and RNA has been developed [50].

3.6 Summary

In this chapter, an electrical model of cell structure was outlined together with the electrolyte-electrode interactions. Detailed operation mechanisms of the electrical double layer between the metal-electrode and insulator-electrolyte were outlined to provide the principles of the charge transfer between the two phases and interface potential development.

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The operation of the ISFET was explained by introducing a site-binding model defining theoretical pH responses for the SiO_2 and Si_3N_4 surfaces. Finally the physical structure of the ISFET was briefly described as an analogue of the MOSFET followed by a Coulter counter architecture. In the next chapter the summary of the design of the integrated sensor system together with readout electronics will be given.

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4 Sensor System Circuit Design

4.1 Introduction

The previous chapter introduced the operating principles for both the Coulter counter and the ISFET, together with a mathematical explanation of how a microparticle modulates the impedance of an electrical sensing zone and an EIS system operation. This chapter focuses on the tools and methods used to develop an integrated Sensor System on Chip circuitry. The two distinct sensor arrays comprise 4 x 4 addressable flow-through pixels, where each of the arrays is complemented with a sensor interface and readout circuitry. Each of the pixels use the two sensors, the Coulter counter and the flow-through ISFET, briefly introduced in Section 3.5. The architectures, and the physical layout design process for both sensors, are verified with appropriate simulations presented in this chapter.

4.2 Analogue/Mixed-Signal System Design

Very large scale integrated (VLSI) circuit design can be differentiated into two distinct categories, analogue and digital. As the technology node[23] decreases, together with the increased complexity of electronic systems implemented on a single substrate, these two overlap hence the term analogue/mixed-signal. Electronic design automation (EDA) software is capable of automating both digital and partially analogue system design based on a behavioural model. Application specific integrated circuit (ASIC) however still requires a "hands on" approach for both the schematic and physical layout design. The integrated circuit uses active and passive components laid out on a common substrate. A component matching methodology therefore is used for design. Furthermore the geometry of the devices is a design specific variable manually controlled by the designer. That feature gives a high degree of freedom in a custom IC design process. A complexity of the custom IC is that it requires a number of tools in the design environment to enable the designer to verify and validate the performance of the ASIC.

4.2.1 Computer aided design

The ASIC design flow involves a number of steps as shown in Figure 4.1. Design practice follows several general steps beginning with a system specification, thereafter is divided into modular blocks (cells) with embedded hierarchy principles. The process is done in a

[23] The smallest feature printed in a repetitive array.

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design environment provided by a set of EDA tools i.e. Cadence Design System. This software package provides a toolset for a front-to-back ASIC design.

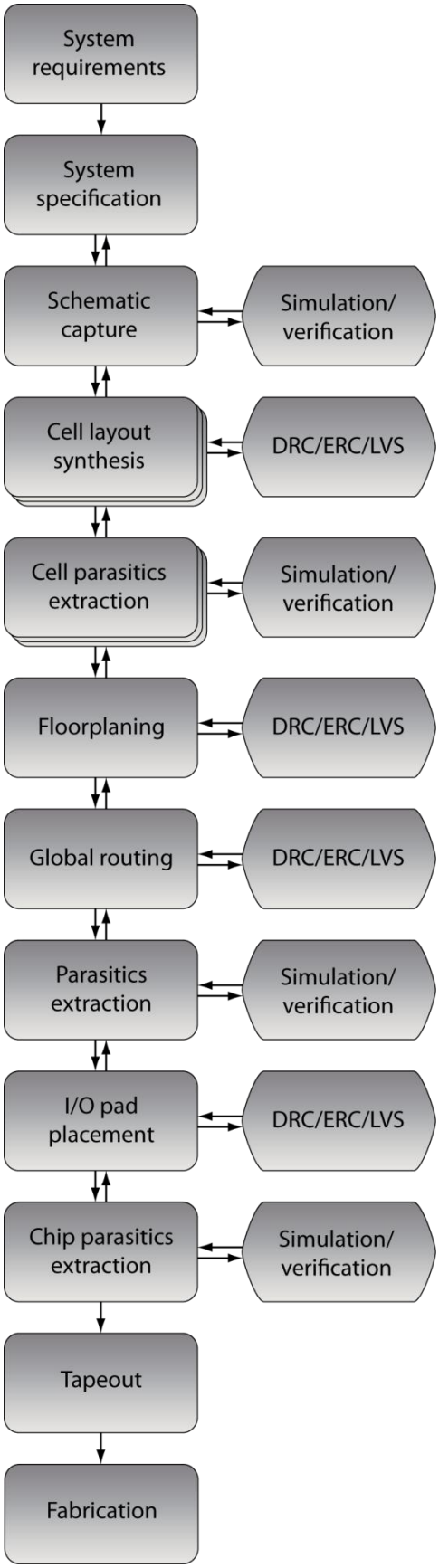

Figure 4.1: ASIC design process flow.

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Initially components and connections in each cell are defined as schematic views in Cadence Virtuoso Schematic Composer. The circuitry simulation and verification is performed with the Spectre Circuit Simulator (derivative of the Simulation Program with Integrated Circuit Emphasis – SPICE [137]), integrated and accessed through the Analog Design Environment (ADE). After successful simulation and verification the physical layout of each cell is designed using schematic-driven-layout (SDL) methodology in the Cadence Virtuoso XL environment. Custom layout editor is used to draw polygons that correspond to the n-type and p-type regions, polysilicon, contacts and metal tracks, using a specific layer (mask) for each primitive component. This task is partially automated by parameterised cell macros that generate layout views for MOSFETs, resistors and capacitors according to given device properties. The layout design is restricted and verified against geometric spacing and electrical constraints for example track length, known as "design rules". Compliance with all these rules is automatically checked using design rule checker (DRC) and an electrical rule checker (ERC) i.e. Assura. Once DRC and ERC rules are successfully applied, the layout versus schematic (LVS) checker is used to compare layout and schematic views to ensure their structural correspondence. This is done by the extraction tool which identifies the combination of layout polygons as devices and generates a netlist. This netlist is compared with the schematic. If successful a complete netlist with back-annotated parasitic resistances and capacitances is extracted. Thereafter it is simulated by a post-layout analysis for more accurate circuit behaviour as it will be fabricated. If successful layout synthesis for each device is completed a chip floorplan is devised and routing between cells is performed. The I/O pads are laid out for an off-chip interface, once the entire chip layout is completed the DRC, ERC, LVS and extraction are done for the entire chip to verify its compliance with the original specification. If agreed the chip design is then ready for tapeout and manufacture.

4.2.2 Process design kit

The design environment requires a set of foundry specific libraries and rules to enable the designer to develop an ASIC. Such a process design kit (PDK) is a set of standard cells for a specific technology provided by the IC foundry service (i.e. *austriamicrosystems* AG (AMS)). AMS provides a design and manufacture service for ASIC and mixed-signal VLSI systems [138]. The 0.35 µm CMOS mixed-signal process was in the scope of the presented work and therefore was used for design and CMOS-MEMS manufacture. This process uses twenty two photolithographic masks during the IC fabrication with a number of a technology specific options [139]:

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- *Core module:* p-type substrate, single polysilicon layer, triple metal layer, 3.3 V CMOS process.
- *Poly-Insulator-Poly (PIP) capacitor module:* p-type substrate, double polysilicon layer, triple metal layer, 3.3 V CMOS process.
- *5 V gate module:* CMOS core module with 5 V MOSFETs with a thick gate oxide (mid-oxide).
- *Other modules:* metal-insulator-metal (MIM) capacitor module, metal four module and high resistive poly resistor module – RPOLYH.

The wafer cross-section (with front-end and back-end layers) used in that process can be seen in Figure 4.2.

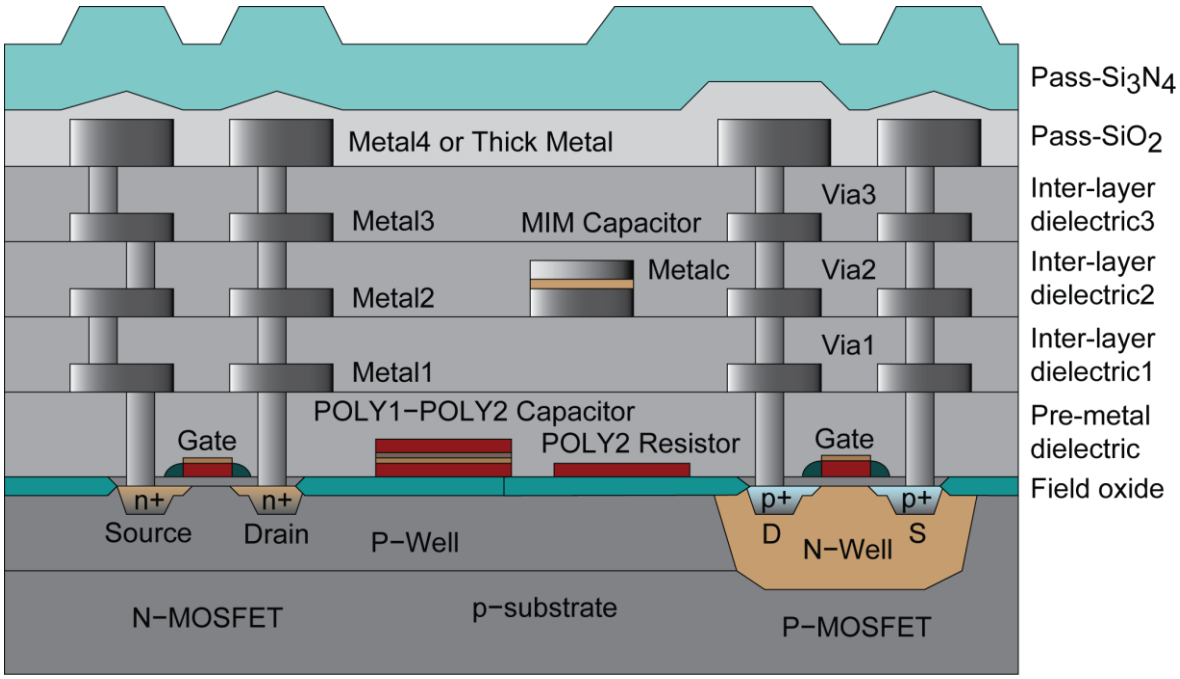

Figure 4.2: AMS 0.35 µm CMOS wafer cross-section [139].

AMS provides a mixed-signal PDK (also referred to as a HIT-Kit) that includes the analogue and digital library cells together with a BSIM3v3[24] and a design rule set. The EDA software, together with the PDK, is used to produce an IC physical layout that complies with the foundry design rules exported to a GDSII[25] format. The *.GDSII file is submitted to AMS for fabrication. Submission to the foundry is performed via the Europractice IC service [140]. This service enables small volume and prototype ASIC design and fabrica-

[24] Berkeley Short-channel IGFET Model third generation version 3.
[25] Gerber Data Stream Information Interchange, it is a database format for two-dimensional graphical designs.

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tion. The service relies on multi-project wafers (MPW) that combines many designs on a single silicon wafer. Therefore reducing the cost of single ASIC to approximately 5–10% of the full wafer cost. After fabrication the ASICs are diced and packaged, however in the a current work naked chips are required for further CMOS compatible post-processing to enable desired device operation as will be discussed in a successive chapter.

4.3 Sensor System on Chip Design

There are two distinct sensor arrays, each equipped with application specific circuitry. Both arrays are multiplexed and addressed independently where a single pixel (micro-channel) is accessed at a time. Sensor specific readout circuitry has been designed to process measured values into voltage and current domains. That enables standard off-chip signal post-processing methodologies and data storage.

4.3.1 Coulter counter design

An equivalent circuit model for the single micro-channel Coulter counter (Figure 4.3) comprises of a the metal micro-electrode in series with the aperture capacitance C_{AP}, EDL capacitance C_I, together with the parasitic components (see Section 3.3.1) and the reference electrode common to all pixels. The electrochemical potential difference between the reference electrode and the electrolyte is represented by V_{REF}. The sensor is connected to the readout circuitry through terminals E_i (subscript i represents the aperture number) and V_{OV}. The on chip metal electrode in represented by its capacitance C_{EL} and resistance R_{EL}. An off-chip reference electrode is an undesirable limiting factor in impedance sensor miniaturisation therefore both impedance measuring electrodes can be implemented on the chip [135].

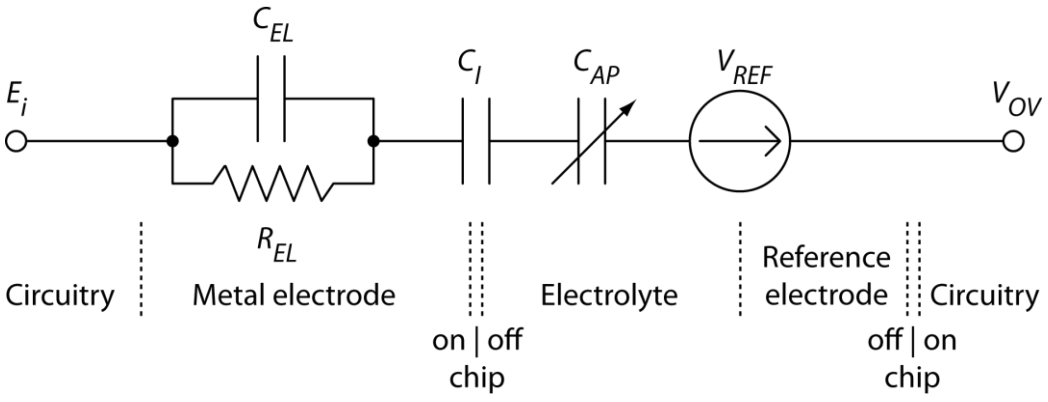

Figure 4.3: Schematic of the equivalent circuit for a single Coulter counter.

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In an analogue ASIC development the fabrication process variability is a major issue thus counter measures are applied during the physical layout design phase. As it is difficult to estimate single micro-pore capacitance, the readout circuitry has to be designed with a large margin consideration to be able to compensate for post-process variation (deep oxide etch non-idealities).

A microparticle or cell flowing through the aperture modulates its impedance. In order to measure the impedance of the aperture, it is crucial to measure current and voltage across the micro-pore. To measure voltage across the aperture, a modified bridge circuit is used (see Section 2.3.1) which will be considered later in this chapter. Its simplified circuit diagram is shown in Figure 4.4. The op-amp used in the design of the bridge circuit is the standard library cell (OP_LN) provided by the foundry [141]. It has a gain bandwidth of 2.32 MHz with load conditions of 50 pF and 1 MΩ.

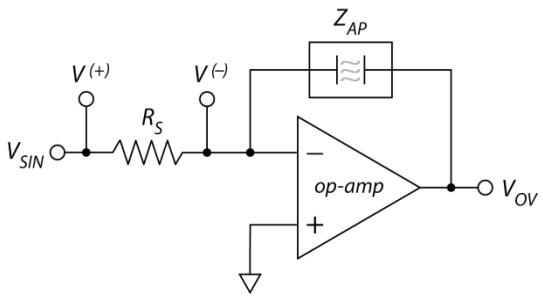

Figure 4.4: Integrator circuit diagram.

Current through the aperture is read by taking a differential measurement across the external (off-chip) resistor R_S using an instrumentation amplifier (i-amp) shown in Figure 4.5. The i-amp circuit topology consists of two stages: input buffer followed by a differential amplifier. Thanks to large input impedance of the two voltage followers the losses in signal integrity are avoided.

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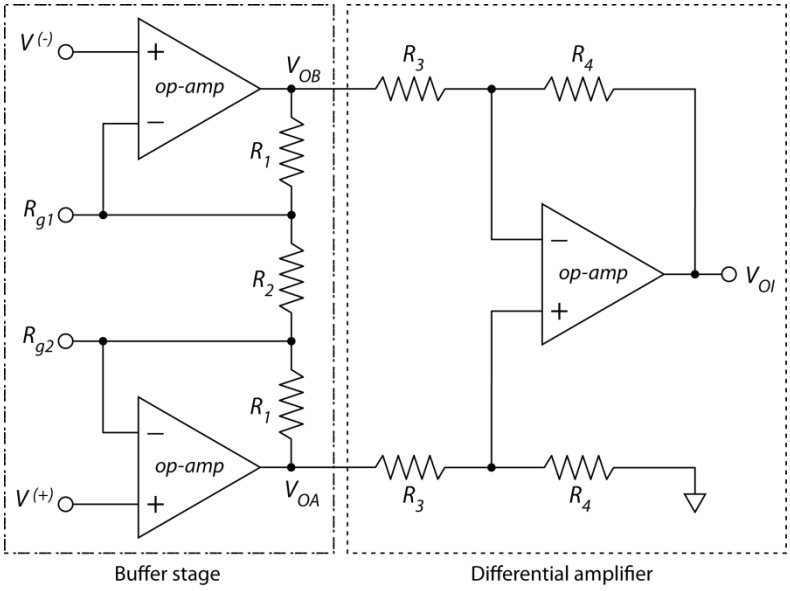

Figure 4.5: Instrumentation amplifier circuit diagram.

Current through R_1 and R_2 causes a potential difference between the low impedance nodes V_{OA} and V_{OB} given by

$$V_{OA} - V_{OB} = \left(1 + \frac{2R_1}{R_2}\right)\left(V^{(-)} - V^{(+)}\right) \tag{4.1}$$

The voltage difference at the input of the differential stage produces corresponding output signal V_{OI} given by

$$V_{OI} = -\frac{R_4}{R_3}\left(V_{OA} - V_{OB}\right) \tag{4.2}$$

Substituting Equation 4.1 into 4.2 produces i-amp gain described as

$$A_{i-amp} = \frac{V_{OI}}{V^{(-)} - V^{(+)}} = \left(1 + \frac{2R_1}{R_2}\right)\frac{R_4}{R_3} \tag{4.3}$$

hence,

$$V_{OI} = \left(1 + \frac{2R_1}{R_2}\right)\frac{R_4}{R_3}\left(V^{(-)} - V^{(+)}\right) \tag{4.4}$$

Current through the aperture can be calculated simply by applying Ohm's law

$$I_{AP} = \frac{V_{OV}}{Z_{AP-i}} = -\frac{V_{OI}}{A_{i-amp}R_S} \tag{4.5}$$

Assuming that gains for the op-amp and the i-amp are fixed and equal to each other, the impedance of the aperture $Z_{AP\text{-}i}$ (with neglected a multiplexing circuitry resistance R_{ON}) is derived from the inverting op-amp theorem given by

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$$\frac{V_{SIN}}{R_S} = -\frac{V_{OV}}{Z_{AP}} \tag{4.6}$$

Where the integrator circuit gain is described as

$$A_{op-amp} = \frac{V_{OV}}{V_S} = -\frac{Z_{AP}}{R_S} \tag{4.7}$$

Substituting Equation 4.5 into 4.6 produces

$$Z_{AP} = \frac{V_{OV}}{I_{AP}} \tag{4.8}$$

In the absence of any additional parasitics (e.g. fringing capacitance between metal layers) the single aperture Coulter counter capacitance is

$$C_C = \frac{1}{j\omega Z_{AP}} \tag{4.9}$$

Terminals R_{g1} and R_{g2} are for the external resistor, to fine tune (program) the i-amp gain if needed in case of the on chip resistors values variation due to the fabrication process.

The op-amps used to design i-amp are the standard library cells (OP05B) [142] provided by AMS in the 0.35 μm CMOS technology PDK. This op-amp has a gain band-width of 2.16 MHz with load conditions of 20 pF and 10 MΩ.

4.3.2 Coulter counter micro-channels array

The array of impedance sensors embedded into micro-pores is constructed as an analog of the random access memory (RAM) architecture. A typical array of memory cells in RAM is accessed through a word line (rows) and a bit line (columns) [69, Chapter 16] which is fed into a sense amplifier for signal read and restore. To access the memory cell a logic address combination is issued to the row and column decoder enabling the desired word and bit line respectively. The column of a flow-through Coulter counter is constructed (Figure 4.6) on that basis, however the row addressing is avoided by using a common off-chip Ag/AgCl reference electrode for all the micro-channels. The reference electrode is used to provide an electrical connection in the feedback loop. This common reference electrode can be avoided by implementing both sense electrodes in the aperture perimeter as it is described in the future work section of this thesis. The complete circuit topology for a 4 x 4 array of an AC Coulter counters, where a $CHANNEL_i$ is the basic building block, is shown in Figure 4.6. The circuit uses a pair of operational and instrumentation amplifiers to output V_{OV} and V_{OI}, while $Z_{AP\text{-}i}$ is modulated by a cell flowing through the micro-channel. The $A_{op\text{-}amp}$ was set to 10 by a fixed resistor R_S of 2 kΩ value, while $A_{i\text{-}amp}$ was set during the IC design process by on-chip resistors also to the value of 10. With the source

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voltage V_{SIN} amplitude set to 100 mV_{pp}, 400 kHz with a 1.5 V DC offset and V_{OFFSET} set to 1.5 V DC, the circuit outputs V_{OV} and V_{OI} are of the order of 1 V for both and are theoretical reference values for the aperture with 0.1 molar NaCl buffer solution (without cells) flowing through.

Each of the apertures is accessed through the analogue demultiplexer *S1* and multiplexer *S2* by logically addressing lines $CSEL_i$ and $\overline{CSEL_i}$ (index *i* states the aperture number). *S1* and *S2* are custom designed cells with a low on-resistance, R_{ON} of 100 Ω, to minimise its influence on the measured signals. Two analogue switches are connected to the impedance sensor in each micro-channel to enable a four-terminal Kelvin measurement configuration (see Section 3.3.1). This configuration allows current to flow through one switch and the voltage to be read across the aperture via a second switch. As a consequence the voltage across the aperture is measured in a more precise way compared to a two-terminal configuration where the signal readout is influenced by EDL parasitic components. The current through the micro-channel is sourced via switch $S1_i$, as $S2_i$ is connected to the inverting terminal of an operational amplifier. This terminal has a high input impedance, hence minimises the influence of the on-resistance of $S2_i$.

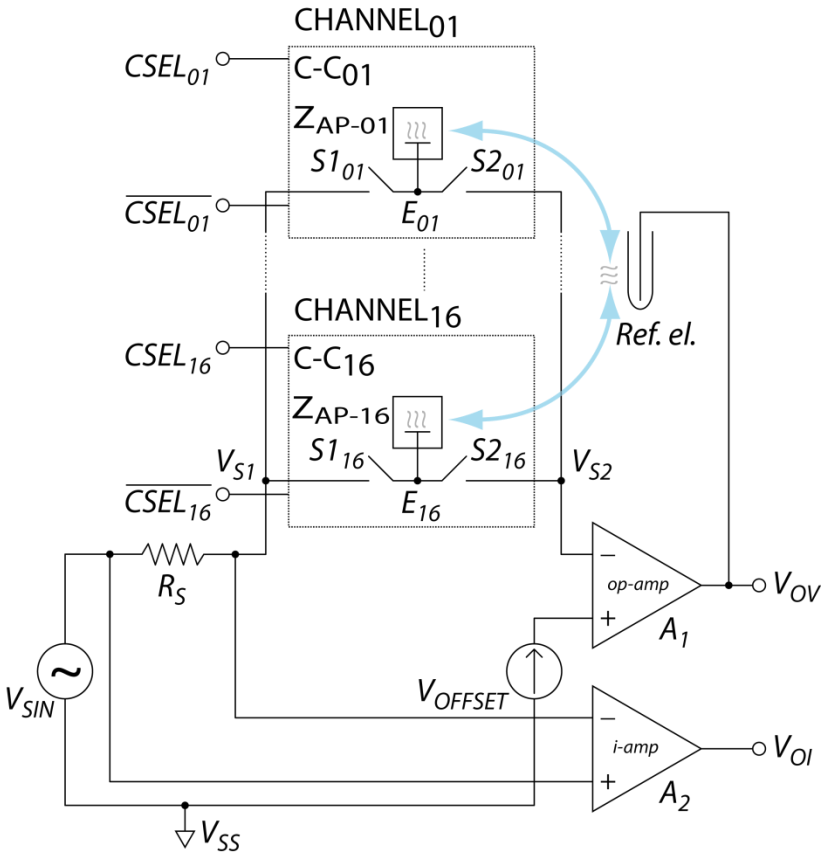

Figure 4.6: Flow-through Coulter counter circuit topology.

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As was introduced in the previous section, amplifier A_1 (op-amp) is used for voltage measurement while A_2 (i-amp) is used for the measurement of the current through the aperture.

The transmission gate (TG), also referred to as the analogue switch, is a basic building block of the analogue multiplexer [143, Chapter 4]. In an analogue signal switching the switch resistance plays a major role, especially in a sensor's signal readout through the TG. For this reason its on-resistance (R_{ON}) is considered during the analogue circuit design. An ideal switch has zero on-resistance and infinite off-resistance however the real switch is constructed utilising a MOSFET device which has its limitations. Basic implementation of a switch uses one n-MOS transistor operating in the triode (linear) region. Switch state is controlled through a gate potential which forms an electrical connection between the input – source and output – drain terminals. In a condition when $V_{GS} \leq V_T$ the n-MOS is off therefore between the input and out terminals an open circuit is formed with a finite but large resistance (~ GΩ). While the gate is biased with V_{DD} and the bulk terminal with V_{SS} the transistors remains in an on-state until the potential at the source and terminals approaches $V_{DD} - V_T$. With this condition the on-resistance increases exponentially and the switch begins to turn off as shown in Figure 4.7 (a). It can be seen that the n-MOS has suitable off and on-resistance however its input dynamic range is limited. The limitations of a single transistor switch are overcome by connecting complementary pairs of n-MOS and p-MOS in parallel. When the control terminal C and its complement $\bar{C}$ are powered with V_{SS} and V_{DD} respectively the n-MOS and p-MOS are off therefore creating an open circuit. In a condition where terminals C and $\bar{C}$ are reversely powered, the MOSFETS are on thus create a low resistance path. Furthermore the dynamic input range of the switch is significantly increased which can be observed by plotting R_{ON} as function of the input voltage (V_{IN}) as shown in Figure 4.7 (b). This graph shows that in the condition when V_{IN} is low, R_{ON} is dominated by the n-MOS resistance. On the contrary when V_{IN} is high, R_{ON} is dominated by the p-MOS resistance. By designing the TG (Figure 4.8) so that the two MOSFETS have the same channel resistance (by selecting an appropriate width and length) the R_{ON} is lowest when $V_{IN} \approx V_{DD} / 2$.

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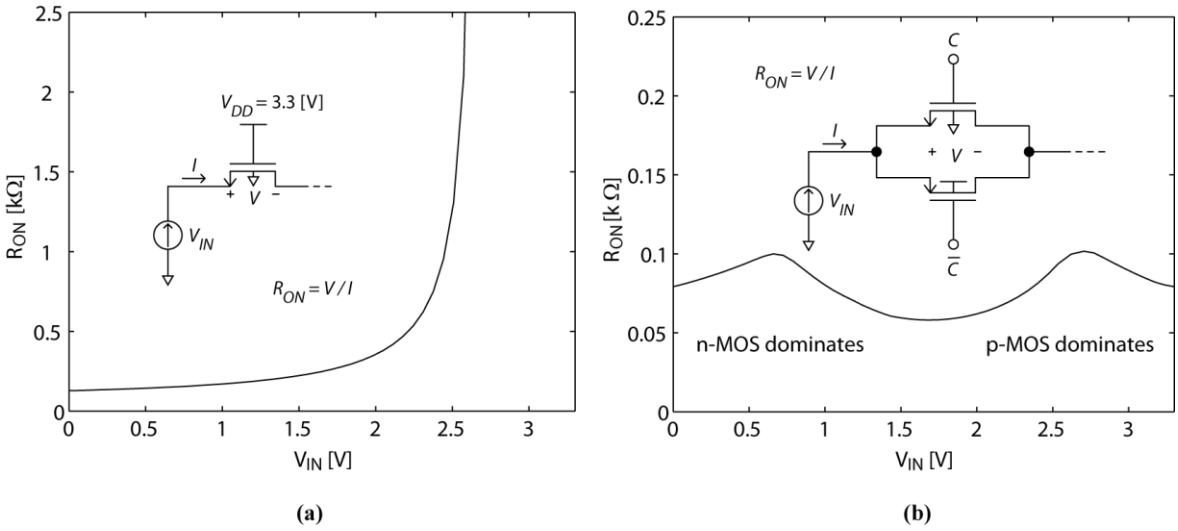

Figure 4.7: The on-resistance of the n-MOS and the TG as a function of the input signal.

The flow-through Coulter counter array is equipped with multiplexing circuitry to electronically address and read signals from the corresponding aperture. Each of the apertures is equipped with two analogue switches $S1_i$ and $S2_i$ (Figure 4.9), both are designed as transmission gates. For a clock feedthrough[26] (charge injection) prevention each of the transmission gates was equipped with dummy transistors D_n and D_p. During the transmission gate design process the optimised values for *W/L* were chosen for the n-MOS and p-MOS transistor and set to 40/0.35 µm and 120/0.35 µm respectively. The corresponding *W/L* for D_n and D_p were set to 20/0.35 µm and 60/0.35 µm.

[26] An undesirable charge transfer from a gate signal to the source and drain regions, it occurs due to the capacitance coupling from the gate to both drain and source terminals.

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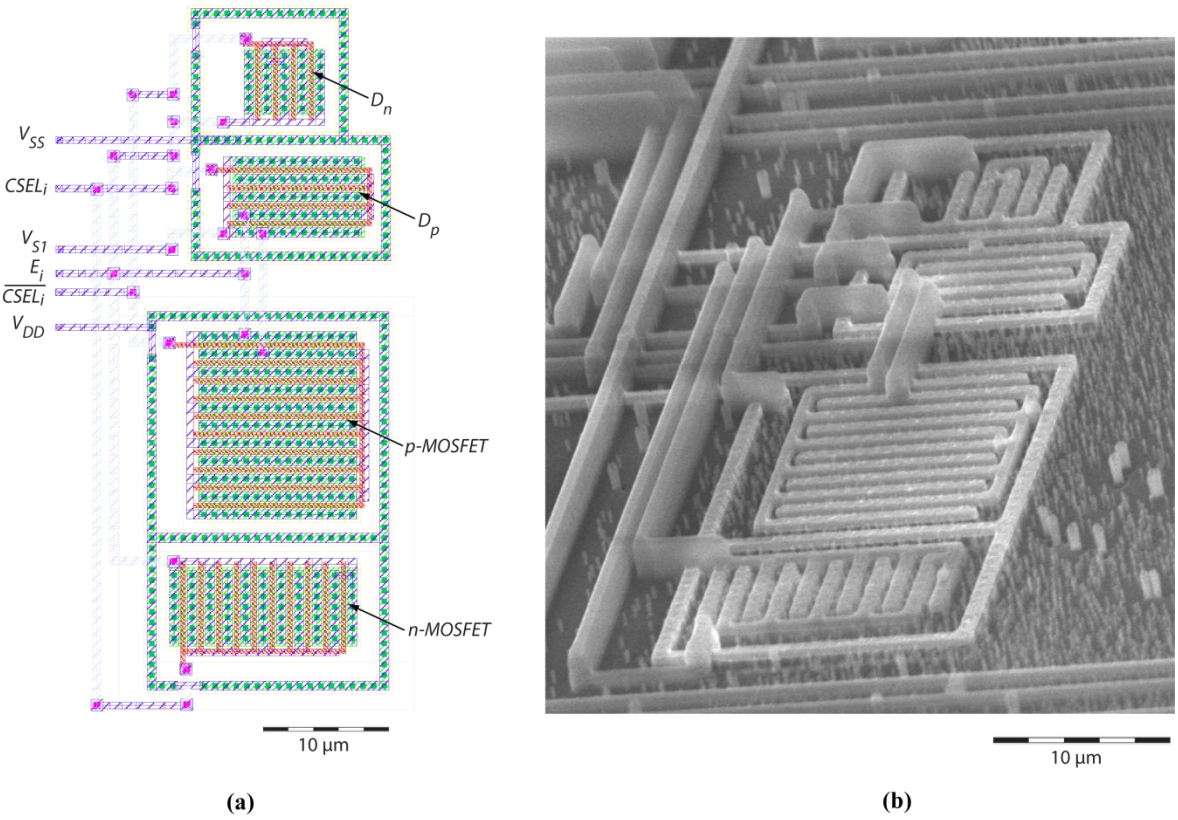

Figure 4.8: Transmission gate (a) CAD layout image (b) scanning electron microscope image.

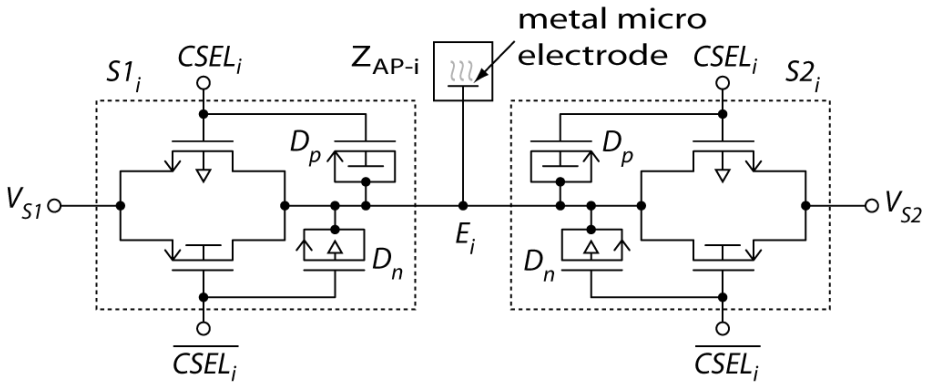

Figure 4.9: Diagram of the Coulter counter pixel circuit.

4.3.3 ISFET design

An equivalent circuit model for the floating gate electrode ISFET (Figure 4.10) consists of the p-MOSFET is series with the EDL capacitance C_I (equivalent of the Helmholtz and Gouy-Chapman capacitances in series). A charge sensitive insulator membrane capacitance C_{INS} and the reference electrode are common to all sensors. V_{REF} represents the electro-chemical potential difference between the reference electrode and the electrolyte solution.

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As for the MOSFET, the ISFET requires a gate potential which is provided through reference electrode connected to a terminal V_G. An ideal reference electrode should provide a low ohmic contact to the electrolyte from which the solution potential is defined and a fixed V_{REF} that does not vary the solution ionic composition. To achieve this the interior of the reference electrode is filled with a reference solution that makes low ohmic contact (utilising a salt bridge) to the electrolyte via an ion permeable pours membrane. The Ag/AgCl and SCE comply with both functions by maintaining an electrochemical equilibrium with the analyte.

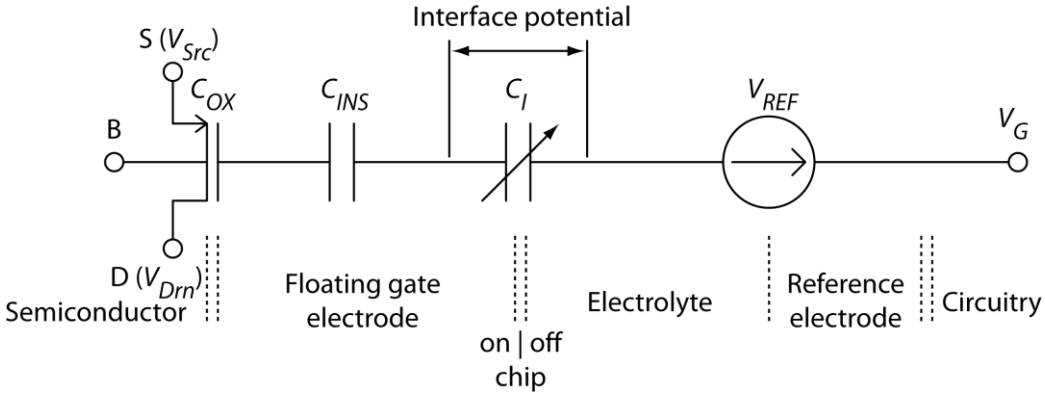

Figure 4.10: Schematic of the equivalent circuit for the ISFET.

The integration of the reference electrode on to a CMOS chip together with the ISFET array has not been yet fully accomplished and is part of on-going research towards further sensor miniaturisation. A standard Ag/AgCl reference electrode therefore is used in presented work common for both a Coulter counter and ISFET array, its bias point however varies according to the sensor used.

The desired transistor type for the ISFET (Figure 4.11) to be based on is the p-MOS. Since the p-MOS is fabricated in an n-type well it is naturally isolated from the main p-type substrate by an n-well-p-substrate reverse biased diode shown in Figure 4.2. This increases the transistors immunity to the noise that can couple through the substrate from the remaining circuitry. A large source of noise on every mixed signal chip is the fast switched digital circuitry. Besides that the ISFET (due to underlying MOSFET) is vulnerable to flicker noise (also known as *1/f* noise) thus at low frequencies this dominates its noise performance [144]. The *1/f* noise in the transistor is generated by a random variation of charge carriers in the channel between the source and drain regions. These carriers are randomly trapped and released in the silicon dioxide. As the potential barrier between semiconductor and insulator carrier band increases, any carrier flowing through the insulator decreases exponentially. There will be a lower number of holes than electrons trapped

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in the oxide due to the barrier experienced by holes in the valence band being greater than barrier seen by the electrons in the conduction band.

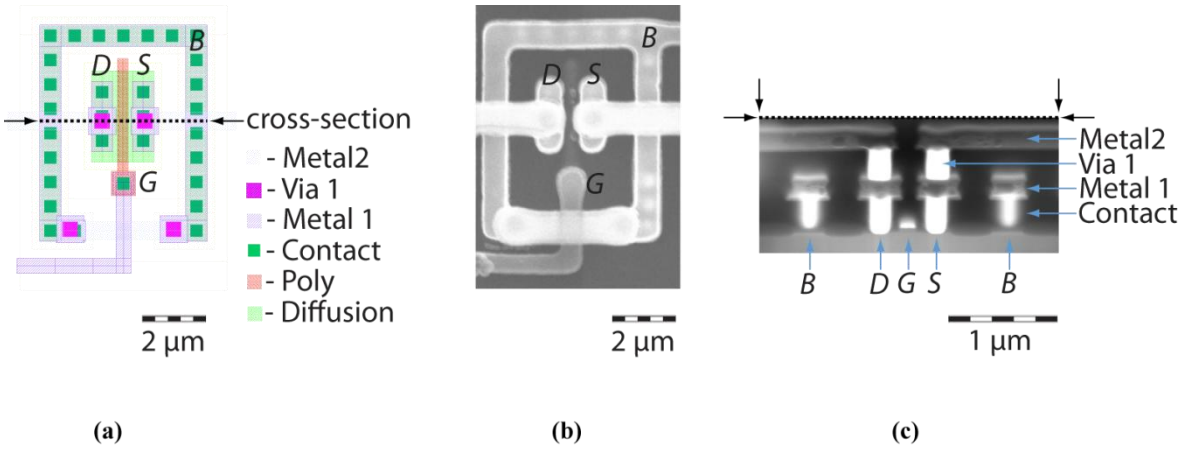

Figure 4.11: The p-MOS transistor used as the ISFET (a) CAD layout image, *D, S, G, B* stand for drain, source, gate and bulk respectively; (b) SEM image - top view; (c) SEM cross-section image.

For this reason p-MOS would have a lower flicker noise than a n-MOS of the same physical shape and size (about 5 times) [145]. The noise level depends on the gate capacitance and is scaled by $1/C_{OX}^2$ [144], thus decreasing the gate dielectric thickness reduces the *1/f* noise. The gate oxide thickness in the AMS 0.35 µm process is of the order of 7.6 nm (typical value) [139], so it will help to immune the ISFET against the flicker noise. The second kind of noise affecting electrochemical measurement using FET based device is the thermal noise (also known as Johnson or *kT/C* noise). This noise occurs due to a random thermal motion of electrons in the conducting medium [143, Chapter 2] and is given by

$$v_{tn} = \sqrt{4kTR\Delta f} \tag{4.10}$$

where v_{tn} is the root mean-square value of the noise voltage, k is Boltzmann's constant, T is the absolute temperature, R is the conducting medium resistance and Δf is the bandwidth. The *kT/C* noise however is well below flicker noise level [144] thus the *1/f* noise mechanism should be considered as the main component affecting the ISFET in a low frequency and DC measurements. It is expected that the total noise level in a presented device will be in the order of a few microvolts which is below the limit that the ISFET can measure.

In an analogue/mixed signal design methodology the device mismatch plays a major role. The preventive practice (device matching principles [146, Chapter 12]) during the design process needs to be applied for lowering of variability. In this design it is important to maximise the gain of the system so that the charge adsorption influence on C_I and minimum size of C_{OX} dominates the system in Figure 4.10. Furthermore it maximises the amount of collected data in each of the apertures. That was confronted with the CMOS

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technology used to design the chip thus the ISFET gate length was set to the minimum value allowed by the technology node. The *W/L* ratio was set to 3/0.35 µm.

The threshold voltage of the ISFET (p-MOSFET) is measured in a condition where the drain current I_D and the source-drain voltage V_{SD} are fixed. A plot of the I-V characteristics for the p-MOSFET with a *W/L* ratio of 3/0.35 µm describes the transistor operation in both the linear (triode) and saturation region (Figure 4.12 (a)). From Figure 4.12 (b) it can be seen that the ISFET operating in the linear region outputs a suitable range values for I_D and V_{SD}. The source-gate voltage V_{SG} therefore is chosen to set the I_D value to 64 µA and V_{SD} to 400 mV as shown in (Figure 4.12 (b)). To get a potential drop of 400 mV with an I_D value of 64 µA requires a resistor with the value of 6.25 kΩ.

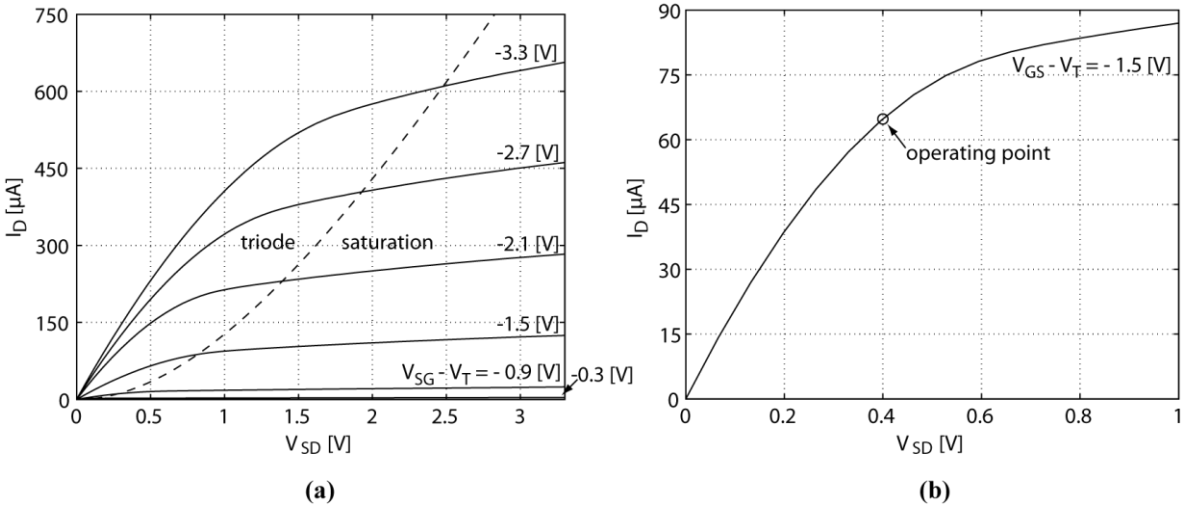

Figure 4.12: Simulation of the drain current as a function of the source-drain voltage.

While the V_T is being modulated by the surface charge adsorption (electrolyte pH) the V_{SG} has to change accordingly to compensate and keep the transistor at a desired operating point. Using a source-and-drain follower circuit (see Section 2.5.1) where the V_G is set by a reference electrode and changes in V_T are followed by the exact (however opposite in sign) variation of source voltage V_S. V_T cannot be measured directly, whereas V_S can. V_S therefore is measured to observe the ISFET threshold voltage modulation due to ionic changes.

The ISFET, like as any other transistor, requires a potential applied to its bulk. While it utilises p-MOSFET (in n-well) the bulk potential V_B has to be connected to V_{DD}. The transistor's V_T however is altered by a potential difference between the source and bulk terminals V_{SB}, known as the body effect [69, Chapter 6]. For p-MOS this is described by

$$V_{Tp} = V_{Tp0} + \gamma_B\left(\sqrt{|2\phi_B| + V_{SB}} - \sqrt{|2\phi_B|}\right) \tag{4.11}$$

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where V_{Tp0} is the p-MOS threshold voltage in a condition where the body is at a source potential, $|2\phi_B|$ is the bulk surface electrostatic potential at threshold and γ_B is the body effect coefficient.

It is necessary to take countermeasures to prevent variations in the V_T due to the body effect, by using a low resistance connection (at multiple points) between the source and the bulk.

4.3.4 ISFET micro-channels array

The array of ISFET based ion sensors embedded into micro-pores is constructed as an analog of the RAM architecture similarly as the Coulter counter array (see Section 4.3.2). The flow-through ISFET array (Figure 4.13) is electronically addressed (column addressing), however the row addressing is avoided. Due to a small number of sensors (16 in total) it will unnecessarily increase resistance and introduce more parasitics into the signal path which is undesirable in a low level DC voltage measurement. The complete circuit topology for a 4 x 4 array of flow-through ISFET based ion sensors where CHANNEL_j is the basic building block is shown in Figure 4.13.

To fix a source-drain voltage of the addressed ISFET a pair of operational amplifiers, A_1 and A_2, with unity gain and resistor R_{SD} (6.25 kΩ) is used. A_1 and A_2 are standard library cells utilised as voltage followers[27]. Two analogue switches are connected to each ISFET with a gate electrode embedded into the micro-channel that enables a four-terminal Kelvin measurement configuration (see Section 3.3.1). In this configuration the current is allowed to flow through one switch while source voltage V_{Src} is read via a second switch. As a consequence the output source voltage for each ISFET_j is measured using a more precise method than with a two-terminal configuration where the signal readout is more influenced by parasitic components. The current (64 μA) through the ISFET_j is provided by a current source via analogue switch S_{2j}. Current flows only through the ISFET_j since the analogue switch S_{1j} connects to the high impedance (non-inverting) input of the A_1, which also minimises the S_{1j} on-resistance. Voltage V_{Src} from the input of A_1 is supplied to the upper terminal of R_{SD}. The current (64 μA) through this resistor is fixed by a current sink, therefore a voltage drop (400 mV) is developed across R_{SD}. Voltage to the node V_{Drn} is supplied by the op-amp A_2 and is followed from its input connected to the lower terminal of the R_{SD}. This circuit configuration maintains a constant source-and-drain voltage V_{SD} in the order of 400 mV, which is in drop-out limits for the both current source and sink. V_{Src} is the output voltage from the system and is directly proportional to the ionic activity in the electrolyte represented in the ISFET's threshold voltage variation. The gate bias V_G for the

[27] Amplifier configuration where the output voltage follows the input voltage.

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addressed ion sensor is provided by an off-chip Ag/AgCl reference electrode that connects to the ISFET charge sensitive membrane via an electrolyte solution.

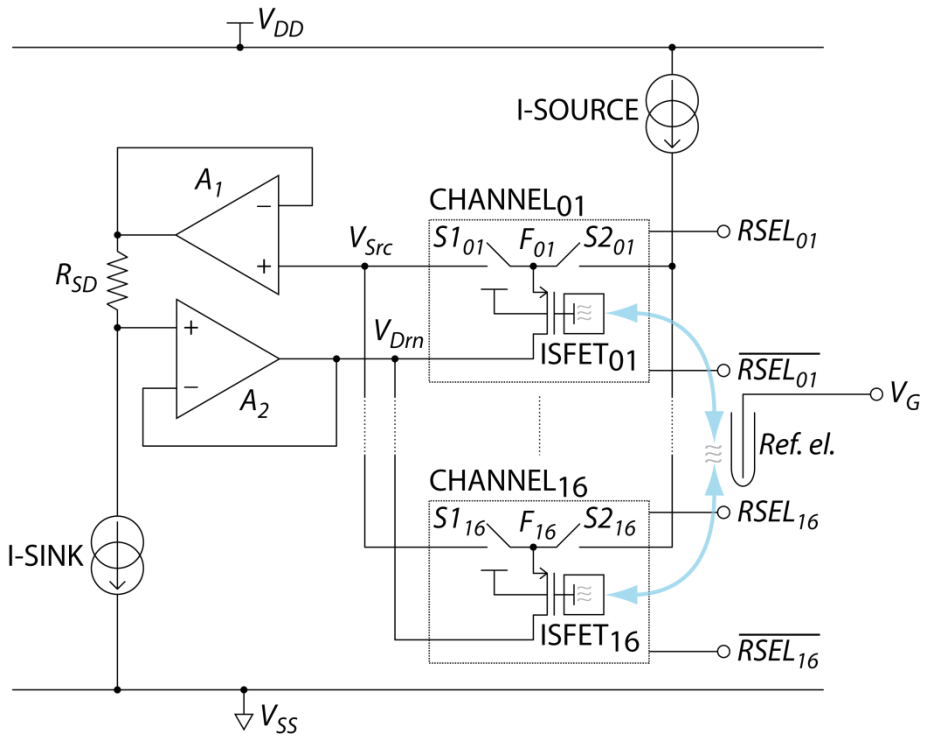

Figure 4.13: Circuit diagram of the flow-through ISFETs.

Each of the ion sensors with a sensing electrode embedded into the micro-aperture side walls is accessed through the analogue demultiplexer *S1* and multiplexer *S2* by logically addressing digital lines $RSEL_j$ and $\overline{RSEL_j}$ (index *j* states micro-channel number) shown in Figure 4.14. *S1* and *S2* are custom designed cells with a low on-resistance R_{ON} of 100 Ω to minimise its influence on measured signals (see Section 4.3.2). Two analogue switches $S1_j$ as the $S2_j$ are connected to the $ISFET_j$ in each pixel to enable a four-terminal Kelvin measurement configuration (see Section 3.3.1).

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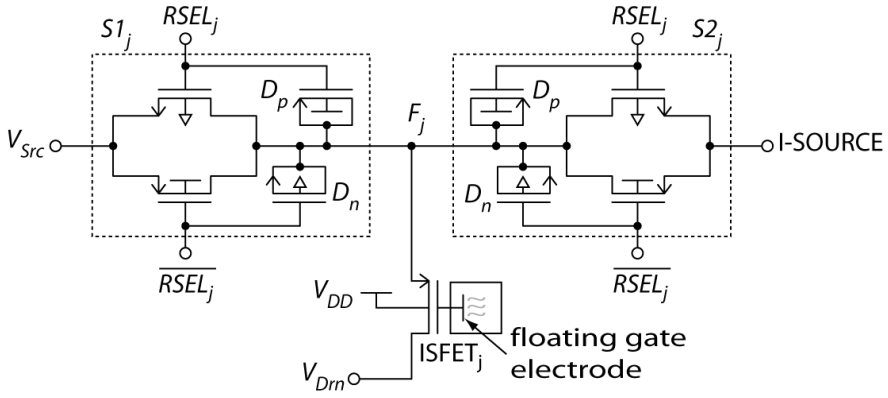

Figure 4.14: Diagram of the flow-through ion sensing pixel circuitry.

4.3.5 Current mirror bias circuits

Current mirror is one of the key components in the analogue circuitry design. Various types of current mirrors (e.g. single, cascode) were developed to suit the needs of the custom ASIC design [147, Chapter 3]. They operate on principle stating that if the gate-source voltage of the two MOSFETs equal in dimensions (*W/L*), their drain currents will also be equal. The basic current mirror circuit using p-MOS transistors is shown in Figure 4.15 (a) where the circuit operates as the current source. The current sink can be constructed using the n-MOS transistors relying on the same circuit topology.

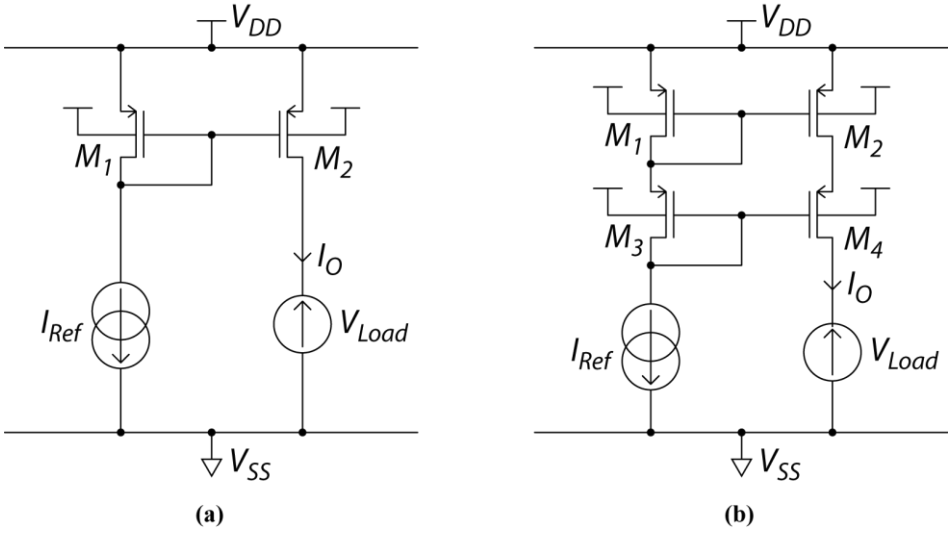

Figure 4.15: Circuit diagram of the (a) basic and (b) cascode current mirror.

The input current I_{Ref} defined by an external current source is "mirrored" by the output current I_O. p-MOS transistors M_1 and M_2 work in the saturation regime where $V_{SD} = V_{SG}$. Therefore using Equation 2.4, the ratio between I_{Ref} and I_O is described as:

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$$\frac{I_O}{I_{\mathrm{Re}f}} = \left(\frac{k_2'}{k_1'}\right)\left(\frac{L_1 W_2}{L_2 W_1}\right)\left(\frac{V_{SG} - V_{T2}}{V_{SG} - V_{T1}}\right)^2 \left(\frac{1 + \lambda\left(V_{SD2} - V_{SDsat2}\right)}{1 + \lambda\left(V_{SD1} - V_{SDsat1}\right)}\right) \tag{4.12}$$

where $k' = \mu C_{OX}/2$ is the process dependent constant, λ is the channel length modulation parameter. For the two transistors M_1 and M_2 fabricated on the common substrate, process dependent parameters k' and V_t will be equal between both devices. The same applies to $V_{SD1} = V_{SD1}$ (omitting the channel length modulation influence), therefore the relation between I_O and I_{Ref} is limited to:

$$\frac{I_O}{I_{\mathrm{Re}f}} = \left(\frac{L_1 W_2}{L_2 W_1}\right) \tag{4.13}$$

Furthermore, the input and output current ratio is a function of the aspect ratio thus controlled within a design process. Consequently it is clear that the M_1 and M_2 having the same W/L ratios will have equal drain currents, thus $I_O = I_{Ref}$. The ideal current mirror has ability to source or sink a constant current independently of an applied load voltage, however in practise this is limited by a finite output resistance and non-zero "drop-out" voltage. The drop-out voltage defines the maximum load voltage value in respect to the supply voltage before a current mirror stops operating. The basic current mirror has large dynamic range however its output resistance is low. To improve that a cascade current mirror is used [143, Chapter 4] as shown in Figure 4.15 (b). The output resistance of this current mirror is well above the sum of output resistances of the M_2 and M_4. An ISFET working in the source-and-drain follower configuration requires fixed drain current. The current source and sink can be utilised as it was demonstrated by Ravezzi and Conci [96].

A derivative of this topology was used to design a "folded" cascode current mirror circuit improving performance while operating with low voltage (3.3 V) supply (Figure 4.16). The current source (mirror topology based on p-MOSFETs) and sink (mirror topology based on n-MOSFETs) are separated to ensure that there is sufficient voltage available for cascode transistors to operate in the saturation region. Instead of active load (diode connected MOSFET) the p-MOS with adjustable gate voltage (via V_{BIAS} terminal) was used to provide the bias current. It also powers down both current source and sink when required, this is achieved by applying V_{DD} to the V_{BIAS} terminal.

The current mirror design requires several iterations to optimise its parameters and make sure (by full circuit simulation) that they fit within the specification required for the measurement system. After the optimisation process the W/L ratios for both types n-MOS and p-MOS transistors are 50/4 µm. To set the source and sink current to 64 µA a potential of 776 mV is needed at the V_{BIAS} terminal as shown in Figure 4.17 (a). The complete current mirror performance is limited by a current source due to its output resistance of 15.7

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MΩ and a drop-out voltage (for 1 % error) of 1.015 V (Figure 4.17 (b)). (The current mirror output resistance was measured for a load voltage sweep from 0.5 V to 1 V).

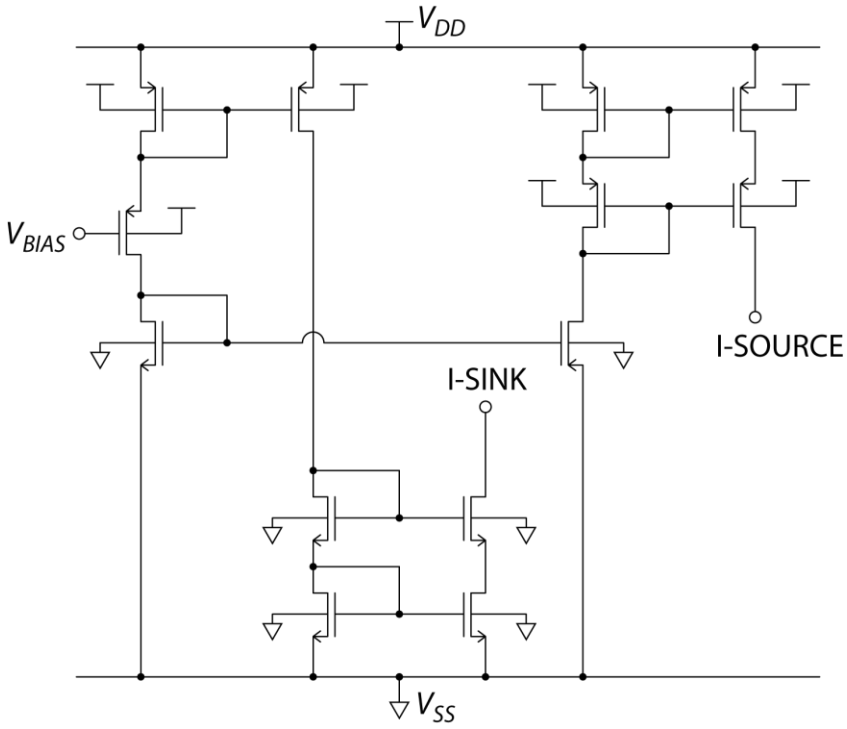

Figure 4.16: Circuit diagram of the current source and sink.

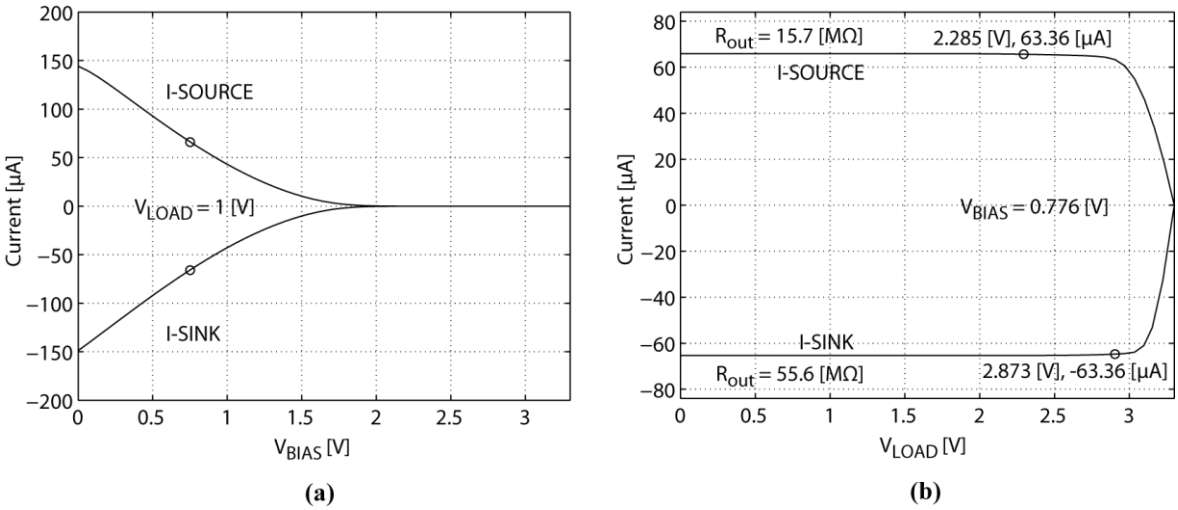

Figure 4.17: Output characteristics for current source and sink. (a) Bias voltage sweep. (b) Output resistance and drop-out voltage.

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4.3.6 Multiplexing circuitry

The two 4 x 4 sensor arrays, Coulter counter and ISFET require appropriate addressing circuitry to be able to read out signal from a desired flow-through sensor. Each sensor array shares common digital logic lines addressing analogue switches. The analogue multiplexers are used for read out the sensor state (see Section 4.3.2 and Section 4.3.4) however these are digitally addressed by the two decoders through digital logic lines separate for each of the two arrays. The multiplexing circuitry block diagrams for the flow-through Coulter counter array and for the flow-through ISFET array are depicted in Figure 4.18 and in Figure 4.19 respectively.

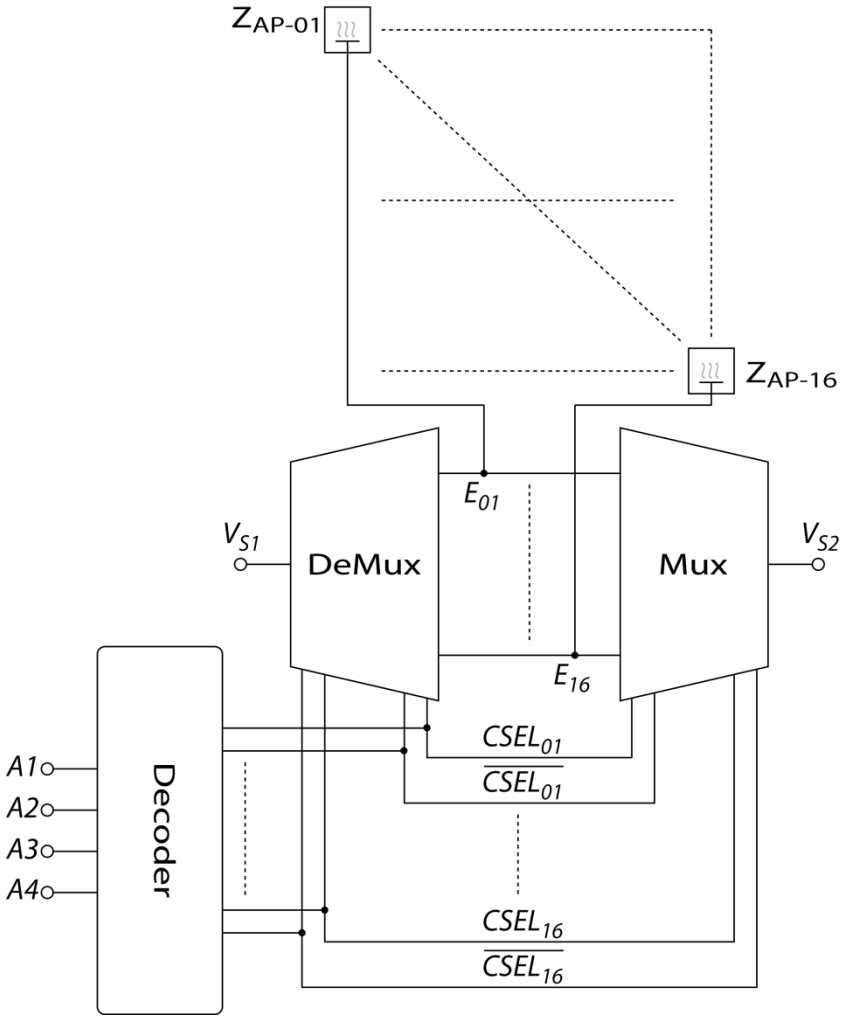

Figure 4.18: Block diagram of the 4 x 4 Coulter counter array addressing circuitry.

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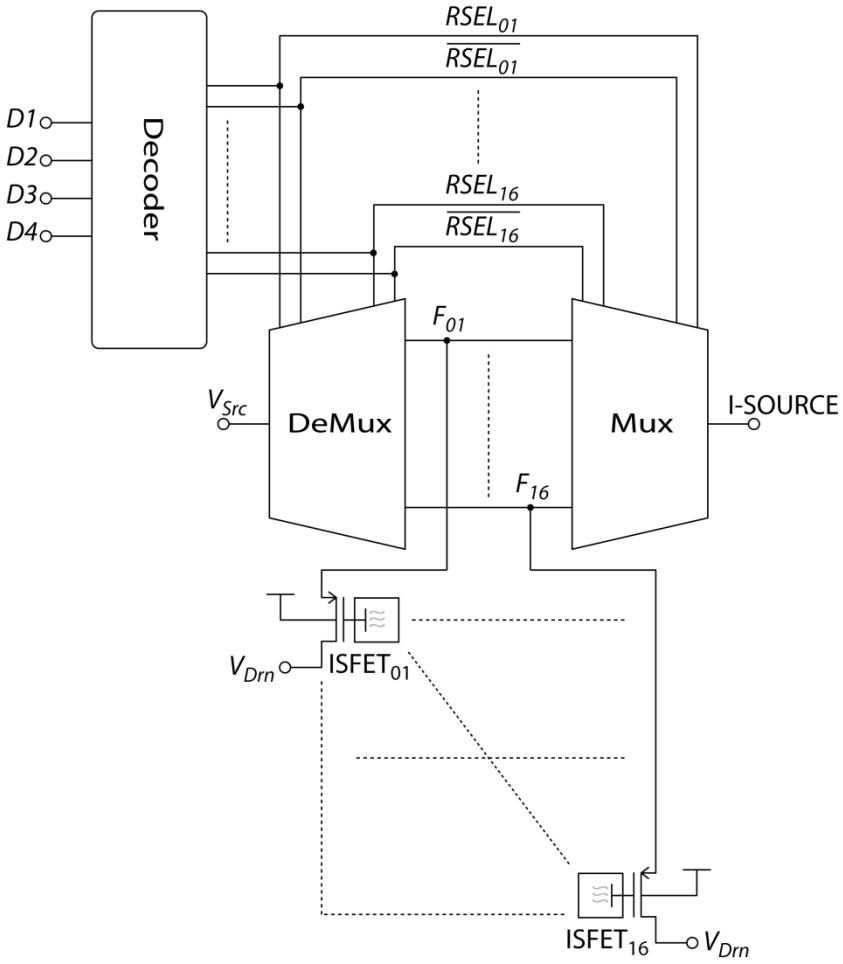

Figure 4.19: Block diagram of the 4 x 4 ion sensor array addressing circuitry.

The decoder receives a predefined combination of bits (logic states) on its inputs (*A1 – A4*) and outputs specified logic states. The basic form of decoder has *n* (number of bits it can receive at a time) logic inputs and 2^n logic outputs. To address sixteen sensors in the array a 4-input-to-16-output decoder is necessary. The four bits input combination is decoded by sixteen logic gates (2^4 = 16). For the given input logic address a complementary pair of logic outputs is enabled (actual output and its negation) according to Table 4.1. Each of the two sensor array has dedicated decoder constructed using 4-input NAND gates (Figure 4.20 (a)) and INVERTERS (Figure 4.20 (b)). The NAND gate and INVERTER are constructed using n-MOSFETs and p-MOSFETs with *W/L* ratio of 0.6/0.35 µm. The analogue multiplexer requires two logic states for each of the transmission gates to be enable, hence the complementary decoder output.

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Channel number	Input address $A_1 \ldots A_4$ $D_1 \ldots D_4$	Decoding function	Outputs $CSEL_{01} \ldots CSEL_{16}$ $RSEL_{01} \ldots RSEL_{16}$
1	0000	$\overline{A1} \cdot \overline{A2} \cdot \overline{A3} \cdot \overline{A4}$	1000 0000 0000 0000
2	0001	$\overline{A1} \cdot \overline{A2} \cdot \overline{A3} \cdot A4$	0100 0000 0000 0000
3	0010	$\overline{A1} \cdot \overline{A2} \cdot A3 \cdot \overline{A4}$	0010 0000 0000 0000
4	0011	$\overline{A1} \cdot \overline{A2} \cdot A3 \cdot A4$	0001 0000 0000 0000
5	0100	$\overline{A1} \cdot A2 \cdot \overline{A3} \cdot \overline{A4}$	0000 1000 0000 0000
6	0101	$\overline{A1} \cdot A2 \cdot \overline{A3} \cdot A4$	0000 0100 0000 0000
7	0110	$\overline{A1} \cdot A2 \cdot A3 \cdot \overline{A4}$	0000 0010 0000 0000
8	0111	$\overline{A1} \cdot A2 \cdot A3 \cdot A4$	0000 0001 0000 0000
9	1000	$A1 \cdot \overline{A2} \cdot \overline{A3} \cdot \overline{A4}$	0000 0000 1000 0000
10	1001	$A1 \cdot \overline{A2} \cdot \overline{A3} \cdot A4$	0000 0000 0100 0000
11	1010	$A1 \cdot \overline{A2} \cdot A3 \cdot \overline{A4}$	0000 0000 0010 0000
12	1011	$A1 \cdot \overline{A2} \cdot A3 \cdot A4$	0000 0000 0001 0000
13	1100	$A1 \cdot A2 \cdot \overline{A3} \cdot \overline{A4}$	0000 0000 0000 1000
14	1101	$A1 \cdot A2 \cdot \overline{A3} \cdot A4$	0000 0000 0000 0100
15	1110	$A1 \cdot A2 \cdot A3 \cdot \overline{A4}$	0000 0000 0000 0010
16	1111	$A1 \cdot A2 \cdot A3 \cdot A4$	0000 0000 0000 0001

Table 4.1: The truth table for the 4-input-to-16-output decoder.

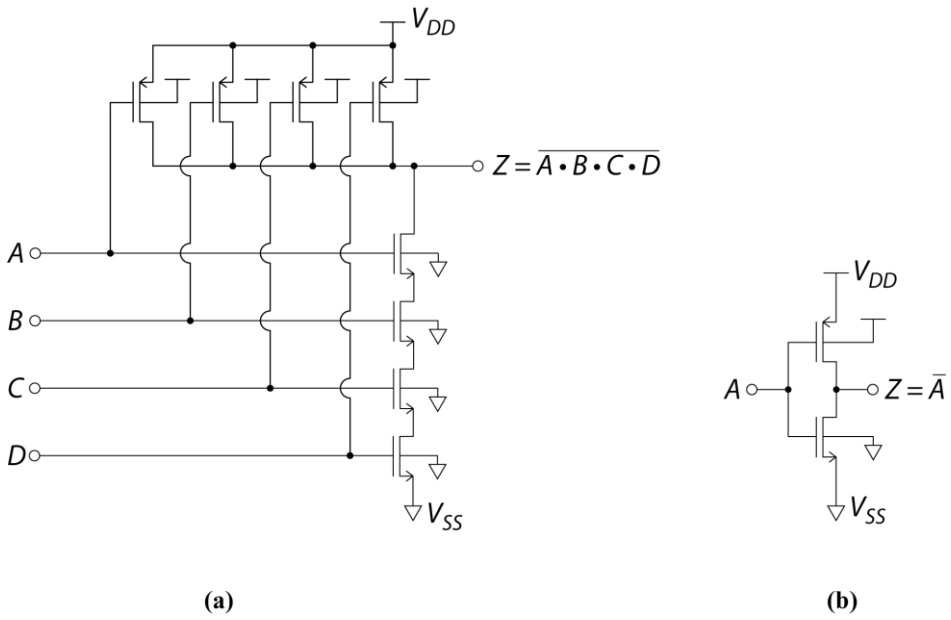

Figure 4.20: Schematic diagram of (a) NAND gate and (b) INVERTER cell.

Digital output from the decoder is fed into analogue single stage multiplexers. The multiplexer is the switching device that allows multiple analogue or digital inputs to be routed to a single output. A simple multiplexer has multiple data-input lines and one output line, be-

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sides that the logic addressing input is required to enable data path from a desired data-input to the common output. Both sensor arrays utilise two multiplexers for each switching circuitry (Figure 4.18 and Figure 4.19).

To enable selected sensor in the array a 16-input-to-1-output analogue multiplexer is required (Figure 4.21). For a given logic address (*A1*. . . *A4* or *D1*. . . *D4*) single data input ($CSEL_{01}$ . . . $CSEL_{16}$ or $RSEL_{01}$ . . . $RSEL_{16}$) is selected in respect to the addressed array according to Table 4.2. Therefore only one analogue data input (E_{01} . . . E_{16} or F_{01} . . . F_{16}) is routed to the multiplexer output (V_{Src} or V_{S2}). The single stage analogue multiplexer is constructed by using sixteen transmission gates (see Section 4.3.2). Each multiplexer requires two addressing signals to enable the desired CMOS switch. Hence a sixteen data select inputs and their complements are fed into each of the multiplexers.

Channel number	**Data select inputs** $CSEL_{01}$ . . . $CSEL_{16}$ $RSEL_{01}$ . . . $RSEL_{16}$	**Data input routed to the output** V_{S2} V_{Src}
1	1000 0000 0000 0000	E_{01} or F_{01}
2	0100 0000 0000 0000	E_{02} or F_{02}
3	0010 0000 0000 0000	E_{03} or F_{03}
4	0001 0000 0000 0000	E_{04} or F_{04}
5	0000 1000 0000 0000	E_{05} or F_{05}
6	0000 0100 0000 0000	E_{06} or F_{06}
7	0000 0010 0000 0000	E_{07} or F_{07}
8	0000 0001 0000 0000	E_{08} or F_{08}
9	0000 0000 1000 0000	E_{09} or F_{09}
10	0000 0000 0100 0000	E_{10} or F_{10}
11	0000 0000 0010 0000	E_{11} or F_{11}
12	0000 0000 0001 0000	E_{12} or F_{12}
13	0000 0000 0000 1000	E_{13} or F_{13}
14	0000 0000 0000 0100	E_{14} or F_{14}
15	0000 0000 0000 0010	E_{15} or F_{15}
16	0000 0000 0000 0001	E_{16} or F_{16}

Table 4.2: The truth table for the 16-input-to-1-output multiplexer.

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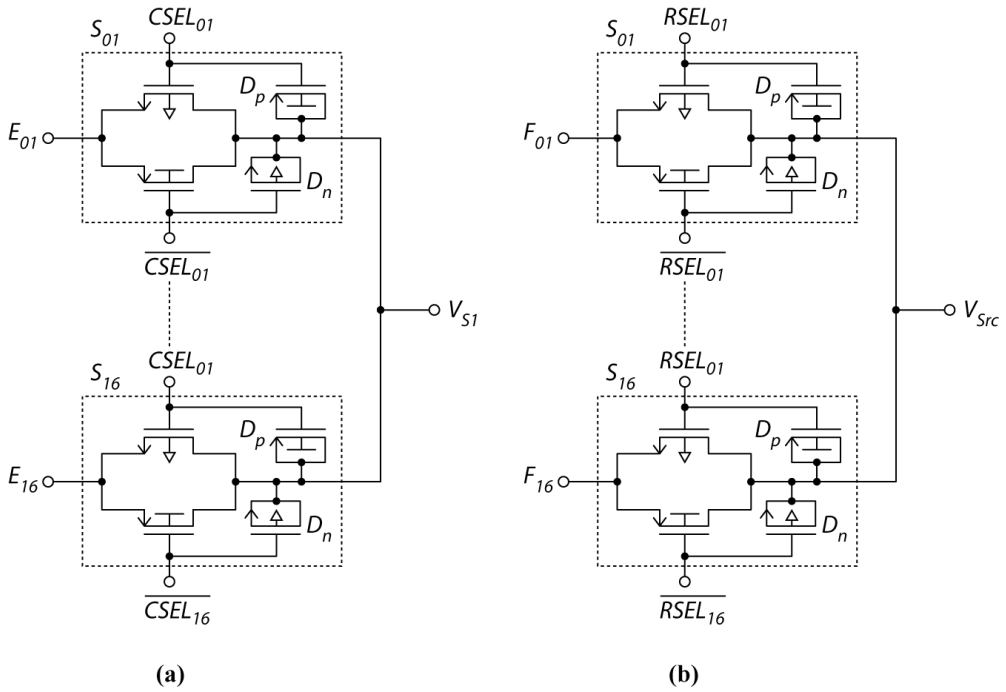

Figure 4.21: Schematic of the 16-input-to-1-output analogue multiplexer used in the (a) Coulter counter array and (b) ISFET array.

4.3.7 Flow through sensor system physical layout

The physical layout of the integrated circuit is defined by drawing a series of polygons on dedicated GDSII layers. Each layer corresponds to a specific step of the CMOS fabrication process. The layout design software has control of most of the layout features within the constraints of a particular technology [139] e.g. transistor's *W/L* ratio is variable according to the need. The technology specific design rules encompass features categorised into four main constraints:

1. Minimum spacing – polygons on a specific GDSII layer must be separated by a minimum spacing (e.g. the minimum spacing is different for the diffusion and metal layers).
2. Minimum length/width – the geometry of the selected layer must exceed the minimum length and width to be fabricated.
3. Minimum density – polygons on a dedicated GDSII layer must exceed the foundry defined density.
4. Minimum extension – specific geometries must extend by a minimum value beyond others polygon perimeters.

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In addition to the fabrication rules detailed above there are also device specific rules such as the “antenna rule”. During certain fabrication processes, such as reactive ion etching, the MOSFET gate oxide is vulnerable to excessive electrostatic charges (ions) that can gather on a large conductive plate connected to the transistor’s gate. This plate behaves like an antenna, increasing the potential difference between both sides of the gate oxide. The gate oxide in a typical 3.3 V CMOS technology can usually withstand a potential difference of several volts (< 8 V) therefore protection against thin oxide break down must be done by limiting the area of a conductive material connected to the gate. Conductors with larger dimensions can be connected to the gate by using pin insertion (connecting to the gate through upper metal layers) or using a substrate diode. EDA tools like Assura (embedded into the Cadence Design System) possess and perform the antenna rule check by default while running the DRC.

The flow-through micro-channel array (Figure 4.22) with embedded Coulter counter and ion sensitive electrode (membrane) in each of the apertures (Figure 4.23) must be specifically designed to enable post-fabrication capabilities and thus sensor operation.

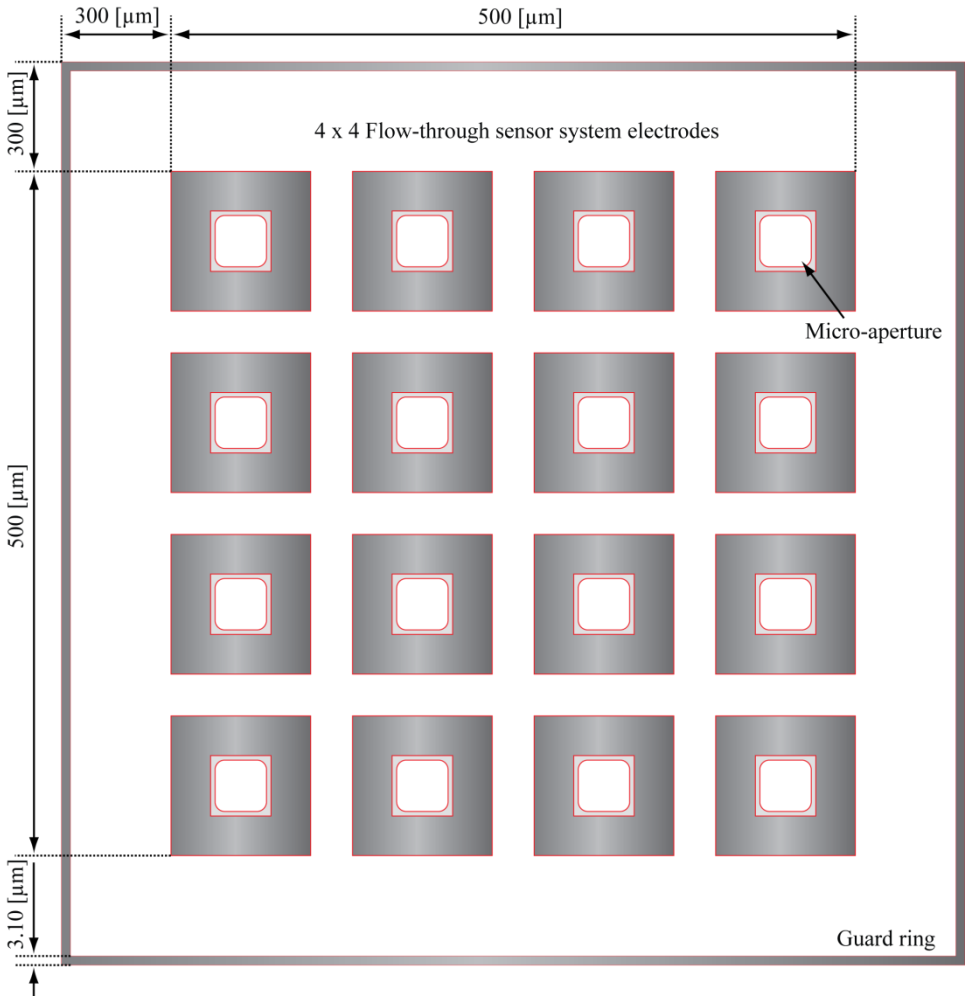

Figure 4.22: Flow-through sensor system electrodes (top view).

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The Coulter counter electrode uses the top metal (Metal 4) layer which is exposed to the analyte solution. Each metal electrode has a square layout area of 100 µm x 100 µm. The inside opening of the metal electrode (A x B) varies from 20 µm x 20 µm to 60 µm x 60 µm, while the pore opening (C x D) varies from 10 µm x 10 µm up to 16 µm x 16 µm Figure 4.23. Therefore the thickness of the ion sensitive membrane t_m (Figure 4.24 (b)) is a variable of (A-C) µm x (B-D) µm. Floating gate electrodes are implemented on Metal 2 so that Metal 1 and Metal 3 work as a screen between the two sensors exposing only the inside perimeter of the ion sensor. Only this perimeter area is influenced by the analyte flowing through the micro-aperture. An ISFET based ion sensor uses the intra-layer-dielectric (ILD) as a charge sensitive membrane made of SiO_2. The array is surrounded by a guard ring to help neutralise trapped charges in the silicon dioxide thus diminish their influence on the ISFET operation.

While in sensing the blood cells diluted in a suspension solution flow through the aperture where the measurement by the two sensors being taken (Figure 4.24 (a)).

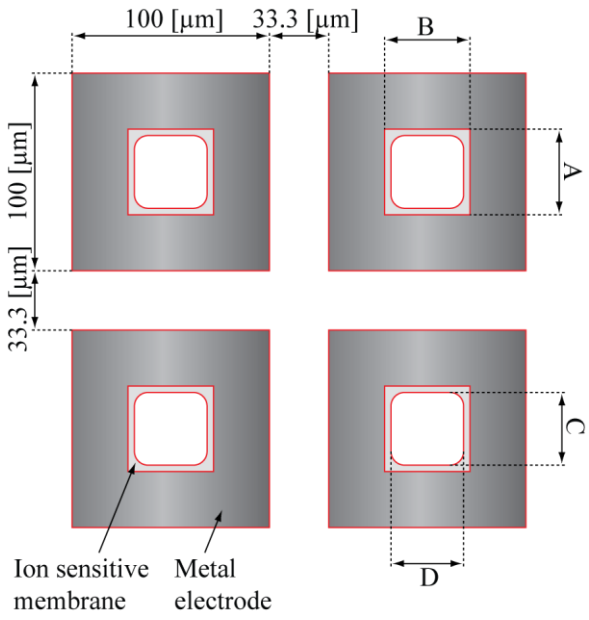

Figure 4.23: Layout of metal electrodes and the ion sensitive membranes.

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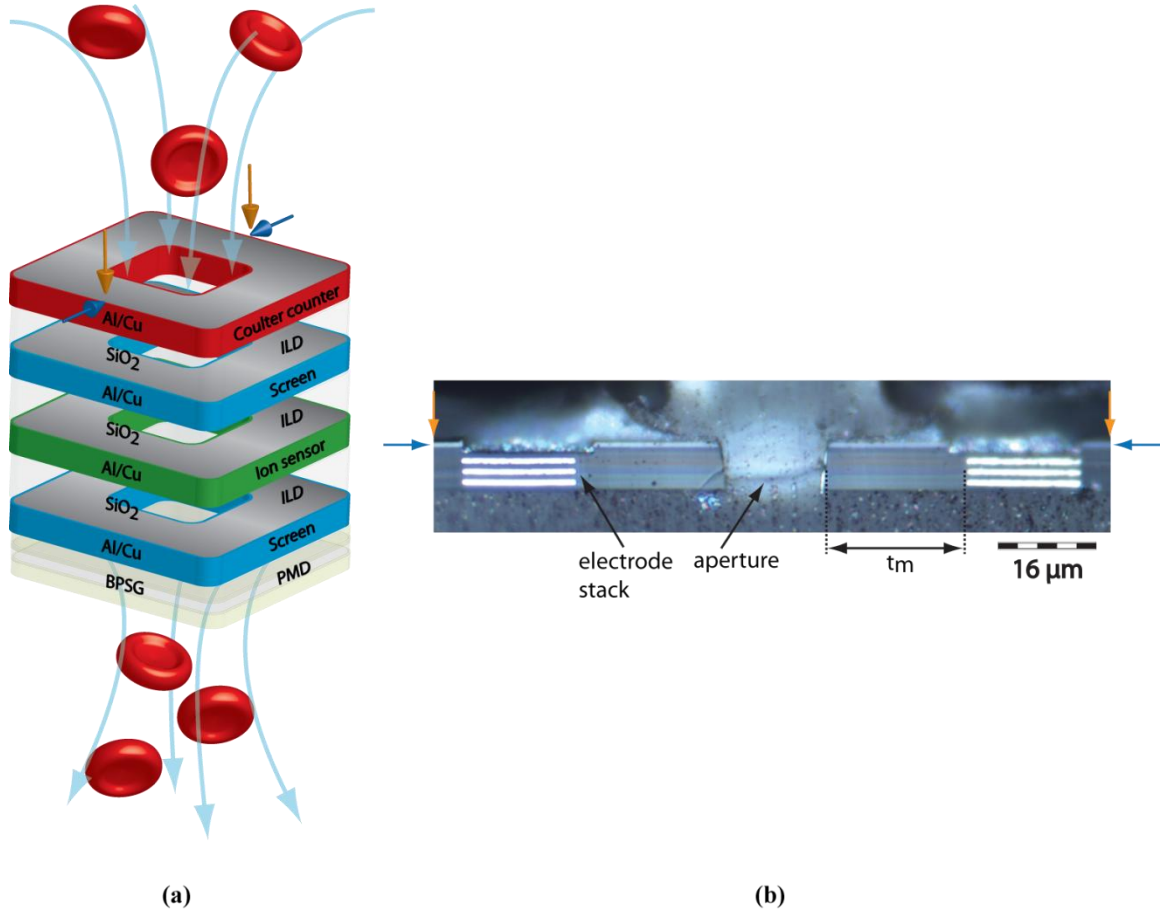

Figure 4.24: Flow-through sensors' electrode stack (a) model image with red blood cells flowing through the aperture, (b) actual microphotograph of the cros-section through the aperture.

4.3.8 Application specific integrated circuit

The physical layout of a chip shown in Figure 4.25 is constructed using both custom designed components and standard library cells provide in PDK. Around the perimeter of the membrane with sensors and core electronics the input-output (I/O) cell (bond-pads) are layed-out creating pad-ring (also referred to as power-ring) to enable interfacing with off-chip electronics through bond wires. During the design process several layout techniques were implemented to reduce noise (by using wire shielding), device mismatch (device matching) and electrostatic discharge (by using ESD protection embedded into the power-ring). Device matching is achieved through a careful device orientation (transistors in current mirrors are oriented in the same direction), symmetry, spacing and physical location on the chip. Sensing circuitry was screened from the digital circuitry using multiple guard-rings (to reduce noise coupling through the substrate) and through laying-out noise sensitive circuitry away from the noisy one. Guard- rings are implemented as low resistance continuous substrate ties providing a low impedance path to V_{SS} for unwanted charge carriers in the bulk. ESD is a serious threat for the core circuitry since electrostatic charges can

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produce potential difference ranging up to several kV. The chip is made immune to ESD by implementing a diode protection circuit. The ESD protection circuitry clamps high potential discharge to the V_{DD} or V_{SS} therefore lowering the voltage connecting to core electronics.

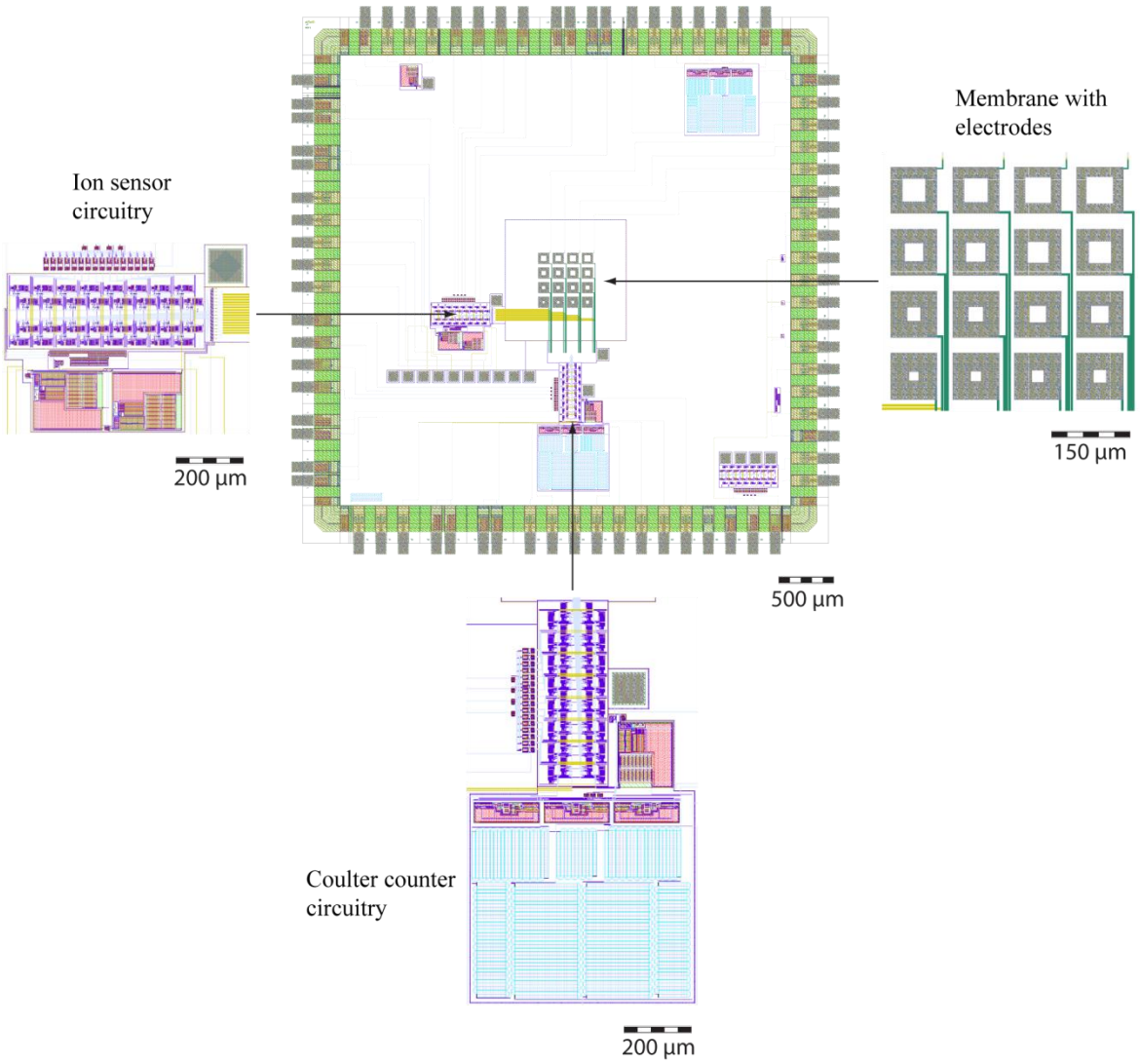

Figure 4.25: Physical layout of the sensor system on chip.

4.4 Summary

CMOS-MEMS (Figure 4.26 and Figure 4.27) was designed utilising the EDA Cadence tool chain. The ASIC with embedded sensor system was developed using the AMS 0.35 µm PDK. The SSoC consists of two 4 x 4 sensor arrays equipped with sensor specific readout circuitry. To maximise chip performance and minimise the chance of failure during post-processing the physical layout was carefully planned achieving the optimum floorplan of the device. Once successfully simulated, a GDSII file was taped out to the foundry. Each

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of the sub-circuits were tested separately for calibration and debugging. The post-fabrication process steps required to open the micro-apertures and enable cytometry will be introduced in the next chapter.

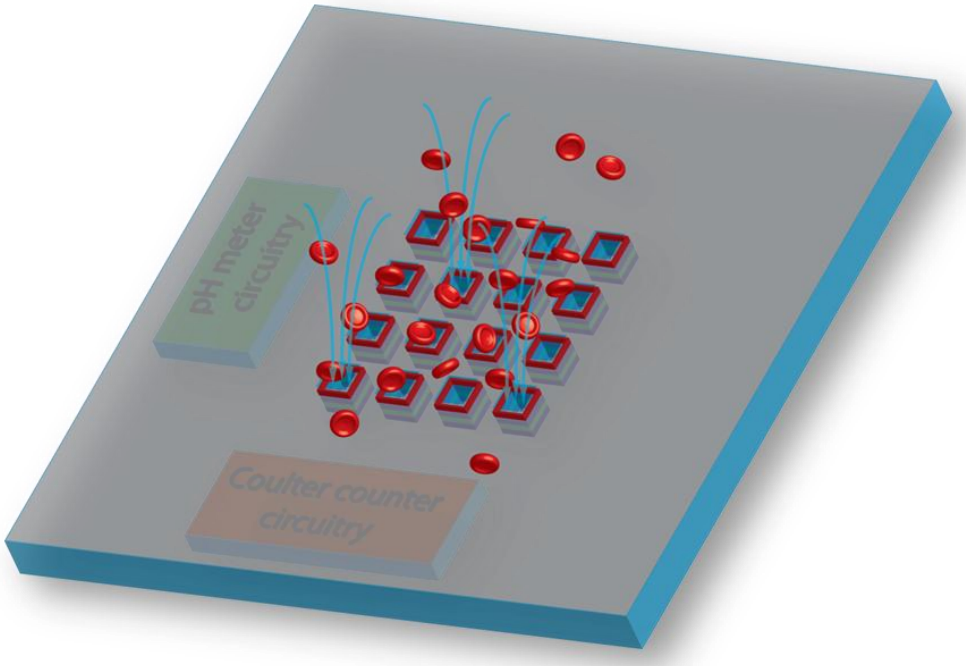

Figure 4.26: CMOS-MEMS cytometry device - model image.

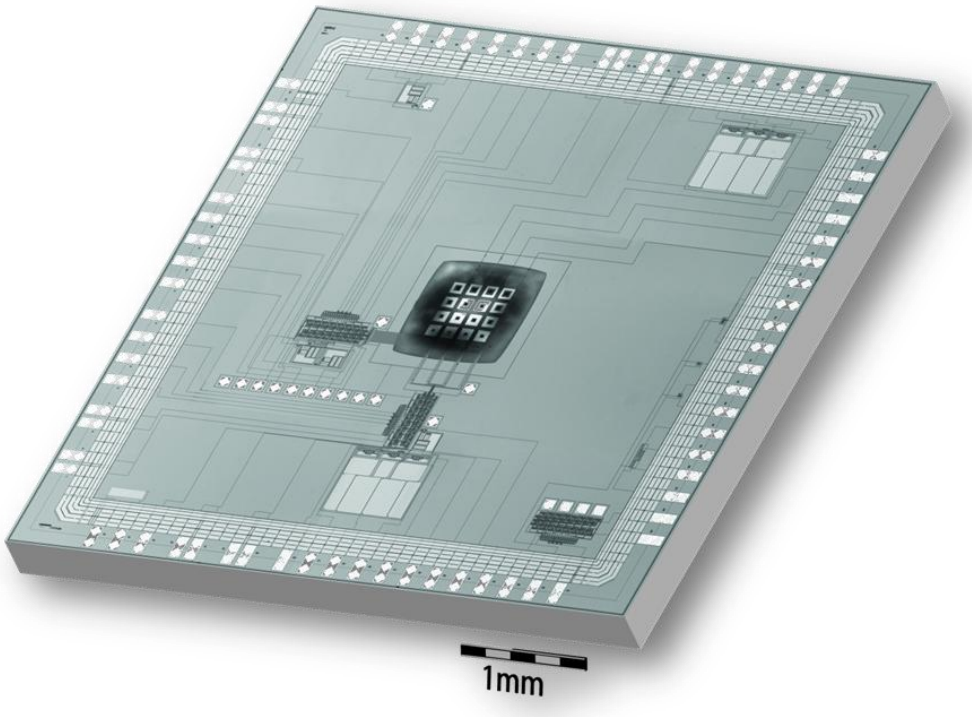

Figure 4.27: Microphotograph of the post-processed SSoC device.

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5 Post-processing and Microfluidic Packaging

5.1 Introduction

The CMOS-MEMS based measurement system design methodology was introduced in the previous chapter together with the sensor system architecture. This chapter encompasses post-processing techniques used to enable the flow-through electrochemical sensor operation, as well as silicon nitride deposition to enhance the pH meter sensitivity. The further sections of this chapter describe microfluidic system development and microfluidic encapsulation in addition to packaging techniques; which are challenging tasks at a silicon chip level.

5.2 CMOS Compatible Post-processing

The CMOS chip has embedded readout electronics for each of the two arrays containing the two distinct sensors; a Coulter counter and an ISFET. The sensor system on a chip consists of the integration of both sensors and electronics on a single silicon dice. However the unpackaged device supplied from the foundry has to be post-processed to enable the flow-through sensor operation. To achieve this three main etch techniques were utilised; reactive ion etch (RIE), deep reactive ion etch in inductively coupled plasma (DRIE-ICP) and focussed ion beam (FIB) milling (see Section 2.4.1).

5.2.1 Front-side post-processing

The post-processing started from the front side, where the micro-apertures were created and then the silicon substrate underneath the array of electrodes stacks was removed. To etch the front side of the CMOS chip a custom deep reactive ion etch process was developed. This enabled standard oxide etch equipment to perform an advanced oxide etch process through all the intra-layer-dielectrics and pre-metal-dielectric (see Section 2.4.1) to finally reach the silicon substrate, which was an etch-stop layer for the front side processing. Due to a layer specific deposition method, properties of the dielectric materials used in the CMOS process vary. The top passivation layer (Figure 4.2), deposited by the plasma enhanced chemical vapour deposition (PECVD) method [148, Chapter 1], is a composition of the two layers of Si_3N_4 and SiO_2. Underneath there are four inter-metal-layer dielectric (SiO_2) layers deposited by PECVD process. The lowest dielectric layer insulating active and passive devices, also referred as the pre-metal-dielectric (PMD) layer, is a stack constructed of the three layers of non-doped silicate glass (NSG), boron-phosphorus doped silicate glass (BPSG) and non-doped silicate glass (Figure 4.24 (a)).

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The PMD layer is deposited by the low pressure chemical vapour deposition (LPCVD) method [148, Chapter 1]. The total thickness of the back-end-of-the-line (BEOL) layers, thus the depth of the front side etch window, was 8 μm [139]. Two very distinct methods were utilised to develop an array of micro-apertures by performing a front side anisotropic etch process. Initially a custom developed reactive ion etch (RIE) process was applied. The etch process requires a photolithographically defined resist mask. To develop the thick resist mask a custom, multiple step photolithography process was developed. The procedure for a multi-layer AZ 4562 (Clariant GmbH) [149] thick film positive photoresist mask development is presented in Table 5.1.

Step	Description
Sample and carrier microscope glass cleaning	1. 5 min acetone ultrasonic bath 2. 5 min methanol ultrasonic bath 3. 5 min isopropanol ultrasonic bath 4. Dry by nitrogen blow
Dehydration bake	1. Sample and carrier glass oven bake at 180 °C for 10 min 2. Cool down at room temperature for 10 min
Carrier glass slide coating	1. Static dispense – coat glass with AZ 4562 resist 2. Stationary – allow resist to flow for 10 s into the corners 3. Spin cycle – ramp up from 0 to 6,000 rpm at 1,000 rpm/s, hold for 10 s and ramp down from 6,000 to 0 rpm at 1,000 rpm/s
Sample attachment	1. Attach the chip in the centre of the carrier glass slide 2. Allow resist relaxation (and solvent evaporation) at room temperature for 10 min
Soft bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 10 min 2. Cool down at room temperature for 15 min
Deposit layer 1	1. Static dispense – coat sample with resist primer 2. Stationary – allow resist primer to flow for 5 s into the corners 3. Spin cycle – ramp up from 0 to 9,000 rpm at 1,000 rpm/s, hold for 30 s and ramp down from 9,000 to 0 rpm at 1,000 rpm/s 4. Static dispense – coat sample and glass slide with AZ 4562 resist 5. Stationary – allow resist to flow for 5 s into the corners and sample sidewalls 6. Spin cycle – ramp up from 0 to 9,000 rpm at 1,000 rpm/s, hold for 30 s and ramp down from 9,000 to 0 rpm at 1,000 rpm/s 7. Allow resist relaxation (and solvent evaporation) at room temperature for 10 min
Soft bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 30 min 2. Cool down at room temperature for 15 min 3. Hold processing for 24 h
Deposit layer 2	1. Static dispense – coat sample and glass slide with AZ 4562 resist 2. Stationary – allow resist to flow for 5 s into the corners and sample sidewalls 3. Spin cycle – ramp up from 0 to 9,000 rpm at 1,000 rpm/s, hold for 30 s and ramp down from 9,000 to 0 rpm at 1,000 rpm/s 4. Allow resist relaxation (and solvent evaporation) at room temperature for 10 min

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Continued from prior page	
Soft bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 30 min 2. Cool down at room temperature for 15 min 3. Hold processing for 24 h to allow resist rehydration
⋮	⋮
Deposit layer 6	1. Static dispense – coat sample and glass slide with AZ 4562 resist 2. Stationary – allow resist to flow for 5 s into the corners and sample sidewalls 3. Spin cycle – ramp up from 0 to 9,000 rpm at 1,000 rpm/s, hold for 30 s and ramp down from 9,000 to 0 rpm at 1,000 rpm/s 4. Allow resist relaxation (and solvent evaporation) at room temperature for 10 [min]
Soft bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 30 min 2. Cool down at room temperature for 15 min 3. Hold processing for 2 h to allow resist rehydration
UV exposure	1. Set the mask aligner UV light source power to 7.2 mW/cm^2 2. Align the resist coated substrate with the pattern on a ferric photolithography mask using front-side alignment mode 3. Single expose for 100 s using modes: hard and contact exposure
Post-exposure bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 10 min 2. Cool down at room temperature for 15 min 3. Hold processing for 20 min
Resist mask development	1. Prepare AZ 400 k developer in 1:4 ratio with RO water 2. Immerse sample in the solution for development for 6 min at room temperature, use continuous and gentle mixing (not ultrasonic) 3. Stop development process by placing sample in the RO water for 2 min 4. Dry by gentle nitrogen blow
Inspection and measure-ment	1. Inspect the resist film for a complete development of the mask windows (inspection needs to be done under a microscope with a UV blocking filter to prevent a further expo-sure thus resist mask damage) 2. Measure mask thickness using surface profiler
Hard bake	1. Oven bake in the nitrogen atmosphere at temperature ramp up at 90 °C for 10 min to 120 °C for 30 min then ramp down at 90 °C for 10 min 2. Cool down at room temperature for 15 min
Inspection and measure-ment	1. Inspect the resist mask under microscope (UV blocking filter not required) for any cracks and non-uniformities that might prevent desirable etch process 2. Measure mask thickness using surface profiler 3. If mask has correct thickness (~ 26 µm) then submit sample for the multiple (6 x 30 min) reactive ion etch process

Table 5.1: Thick film AZ 4562 photoresist multi-layer development procedure.

The photolithography process is started by a cleaning the sample in the ultrasonic solvent bath for removal of surface impurities, followed by a dehydration bake at 180 °C. It was important to use non-metal tip tweezers while sample handling to prevent resist scratching. In the next step the sample was attached to a 22 mm x 22 mm borosilicate glass

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slide for handling and processing improval. The attachment was done by spin-coating the glass slide with AZ 4562, placing sample in the centre of the glass and baking a 90 °C for 10 min. To achieve an etch depth of 8 μm using RIE, the resist mask has to be firm to withstand the etch process and prevent physical damage to the unexposed areas. During the test runs etching Si_3N_4 and SiO_2, the selectivity for AZ 4562 resist was defined to be 1:3 (the resist was etched three times faster than the substrate). Therefore the resist mask needed to be over three times thicker (> 24 μm) than the etched Si_3N_4/SiO_2 substrate. That was achieved by depositing six layers of a thick film AZ 4562 photoresist mask on the sample. Deposition of a resist mask of that thickness on a substrate of 5 mm x 5 mm in dimension, encountered significant obstacles during UV exposure. Using a single layer of the thick film resist (> 10 μm) the UV light could not uniformly penetrate the mask window the full depth due to a semi-transparent resist layer. This was later linked to a thick film mask property (varied with a mask depth) due to a non-uniformity arising along resist thermal processing (baking and cooling). The second problem with a single layer thick mask depositing on to a small substrate is a significant increase in the film thickness in the edge around the perimeter of the sample, known as the edge bead error. The edge bead was developed by a build-up of the resist around the outer edge of the substrate caused by fluid surface tension during the spin-coating process. To prevent both the edge bead and the single layer thick film exposure problem, the resist mask was deposited as a number of approximately 4.5 μm thick layers spin-coated at a high speed. After the dehydration bake and appropriate cooling down to room temperature the sample was attached to the glass slide. Then the resist primer (adhesion promoter) was applied on the sample and spin-coated at 9,000 rpm using 1,000 rpm/s acceleration and de-acceleration speed, thereafter the first layer of resist was deposited. AZ 4562 resist was applied on to the substrate from a syringe equipped with a filter to prevent impurities and air bubbles in the mask. Since the AZ 4562 resist has a high viscosity it requires some time to flow on the sample surface and sidewall for uniform coating, five seconds was allowed for that purpose before spinning. The spin cycle was carried out using a programmable resist spinner, PWM32 (Headway Research, Inc. Texas USA). During the test runs it was found that spin-coating a 5 mm x 5 mm sample with AZ 4562, the resist produced a 4.5 μm thick layer after spinning at 6,000 rpm however the edge beads were still of significant height. Therefore the spin speed was increased to 9,000 rpm which significantly reduced edge beads while producing a mask thickness of 4.5 μm. While developing the mask on the actual sample the spin cycle process was divided into three sequences: ramping up the spin speed from 0 to 9,000 rpm with 1,000 rpm/s acceleration, actual spinning at 9,000 rpm for 30 s and ramping down the speed to 0 rpm with 1,000 rpm/s de-acceleration speed. This further reduced the edge

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beads producing a uniform and flat mask surface. After spin-coating the sample was left at the room temperature for 10 min to let the solvent evaporate from the film, and let the resist molecules rearrange (resist relaxation). Thereafter the sample was baked in the convection oven in a nitrogen atmosphere at 90 °C for 30 min. There was a significant difference in the baking process when using a hotplate and an oven. In the oven the sample is exposed to a constant temperature from all sides, while using a hotplate exposes the sample to the desired temperature only from one side and the other sides are cooled at room temperature. For that reason it was important to oven bake the sample attached to the glass slide. After the sample was retracted from the oven, the cooling down process at room temperature was also important: it had to be carried out carefully to prevent cracks in the resist mask (the sample should not be touched directly but only handled through the carrier glass slide). At this point the first mask layer processing was finished and resist deposition was stopped for 24 hours to allow resist rehydration. The rehydration process is necessary to re-establish a certain water content in the resist which was evaporated during the soft bake step. Appropriate water content in the AZ 4562 positive photoresist is required to allow a reasonably high development rate and a high contrast. That water content has to diffuse from the air into the resist film, therefore a time delay is required after each soft bake process. The following resist layers were spin-coated until layer six, however the resist primer deposition was omitted since it was only required for layer one to increase adhesion between the Si_3N_4 substrate and the AZ 4562 photoresist. Once the sixth layer was deposited the rehydration process was carried out for two hours at room temperature. Thereafter the UV exposure was done through the photolithographic 2.5 inch ferric mask. The front-side coating and photo resist mask development process can be seen in Figure 5.1.

The photolithographic masks for the front and back-side post-processing were designed in Cadence Virtuoso, once signed off the original pattern was written on the master 4 inch chrome mask (on glass substrate) by electron beam lithography, Leica EBPG 5 HR 100 (Leica Microsystems, Germany). The front side etch photolithography mask was designed as an array of circular openings with diameters ranging from 10 to 50 μm to avoid problem with sharp corners while the resist mask development. The square features with sharp corners tend to round while thick film resist processing (during bake step). Front side etch mask was also equipped with markers for the back-side alignment (Figure 5.2). Since the 4 inch master chrome mask contained multiple patterns had to be later reproduced to have each pattern separately on the 2.5 inch ferric copy mask.

Single UV exposure was done for 100 s using a mask aligner (MA6, SUSS MicroTec) in front side alignment mode, and equipped with a UV light (400 nm wavelength) source (mercury lamp) to write a mask pattern on to the positive AZ 4562 photoresist film.

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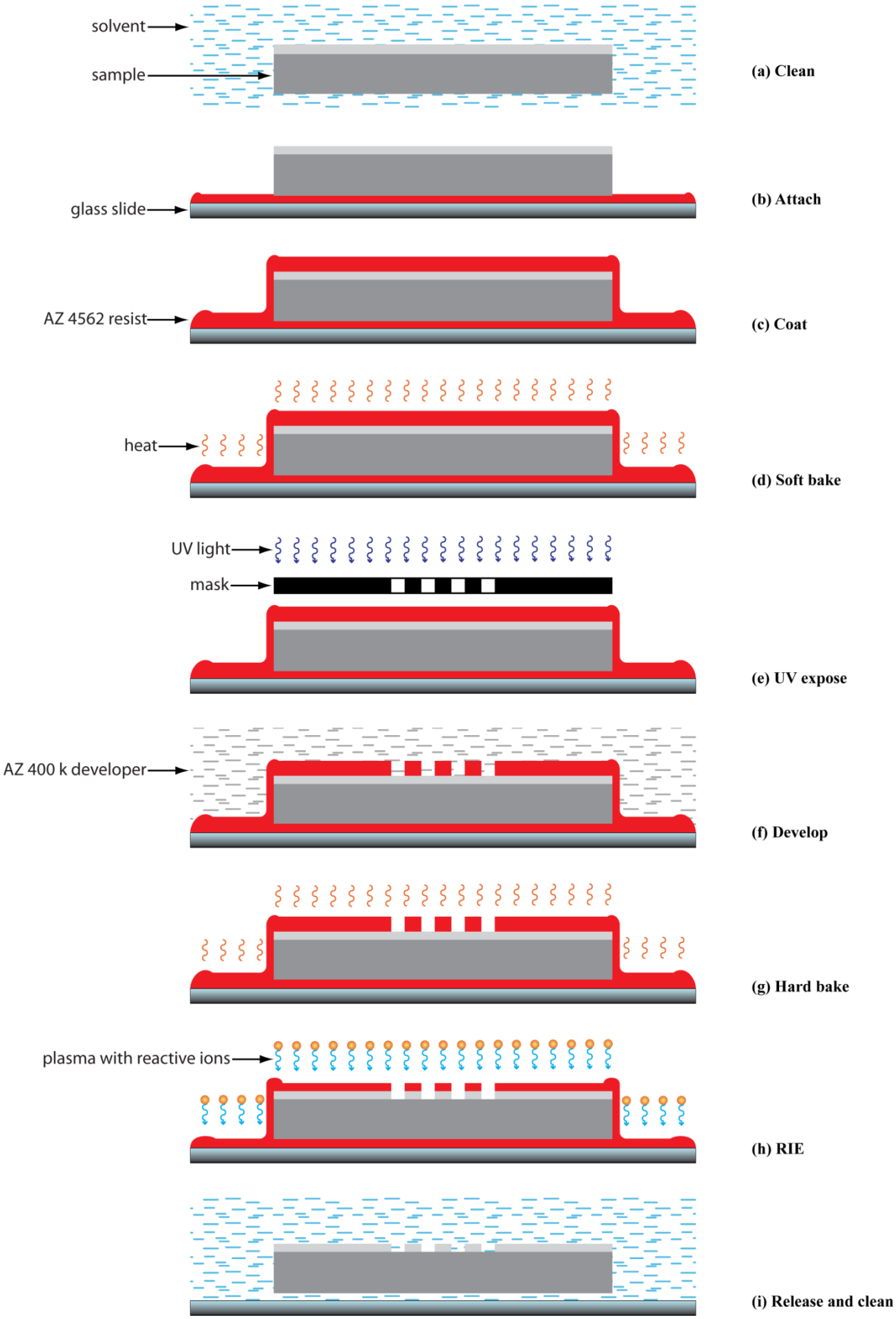

Figure 5.1: Front-side coating process flow.

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The UV exposure time was fine tuned to avoid resist mask overexposure, this prevented a rough mask window profile and bubbles in the resist due to an excessive nitrogen molecule (N_2) formation. The N_2 formation is the result of photo active compound diazonaphtoquinone (DNQ) conversion into an indene carboxylic acid, with the N_2 being a side product of this reaction. In the post-exposure bake process, thermally activated N_2 content diffuses into the resist surface and dissipates.

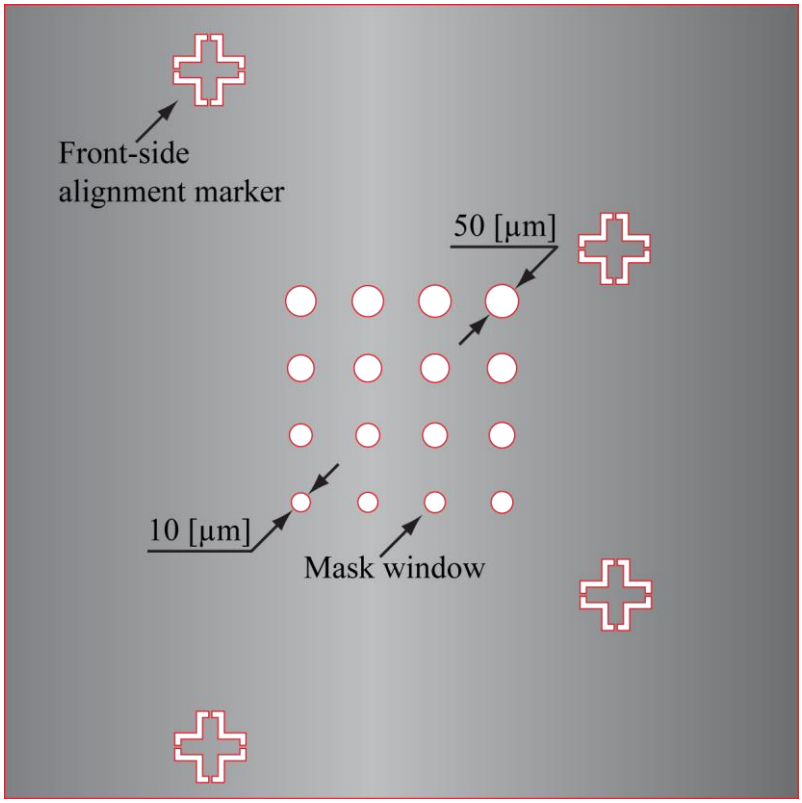

Figure 5.2: Front-side photolithography mask.

Once exposed and baked a 20 min delay was allowed before the resist development process. The resist mask was developed by immersing a sample in the AZ 400 k developer [149] in 1:4 ratio with RO[28] water solution. The process was carried out at room temperature for 6 min after which the reaction was stopped by placing the sample in the RO water and then dried by nitrogen blow. To assure complete development of all the mask windows, the sample was inspected under the optical microscope equipped with UV blocking filter to prevent further exposure. The mask thickness was measured using a surface profiler, Dektak 6M (Veeco). The six layers of AZ 4562 resist deposited on to the substrate developed a 27 µm thick mask. To strengthen the resist film the hard bake was performed in a convection oven. At this point the six layer mask can crack due to a rapid temperature

[28] Reverse osmosis – filtration process that removes large molecules and ions from water.

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change. Therefore, the temperature was ramped up from room temperature to 90 °C for 10 min, then the sample was placed in the oven at 120 °C for 30 min, ramped down to 90 °C for 10 min and finally cooled down at room temperature for 15 min. This process reduced the internal stress of the multilayer thick film resist mask. After hard bake the sample was inspected once again for cracks, and the mask thickness was measured. The total film thickness of 26 µm (after hard bake) was enough to reach a desired Si_3N_4/SiO_2 etch depth of 8 µm with a selectivity ratio of 1:3. At this stage sample was ready to submit for RIE process.

The RIE process was performed in Plasmalab 80 Plus (Oxford instruments, UK) system using a custom developed and optimised etch recipe. Multiple etch runs were required (6 x 30 min) since the machine had to be cleaned after each 30 min of processing. The dry etch process uses chemically reactive plasma to remove material in the resist mask window opening. Once the sample is loaded into the etch chamber, the plasma is generated by an electromagnetic field. High-energy ions generated in the plasma are accelerated towards the sample. These react with the surface achieving a highly anisotropic profile. Due to its anisotropy the RIE is often used to etch oxide layers on the CMOS chip [150]. The etch process used a sulphur hexafluoride (SF_6) and argon (Ar) gaseous mixture composition in which the plasma was generated. The exact Si_3N_4/SiO_2 etch procedure using RIE can be seen in Table 5.2.

The etch process was initiated by an O_2 ash to remove impurities from the etch windows that could lower the etch rate. Thereafter the dry etch process was performed multiple times. After each run the sample was inspected for any damage to the resist mask that may cause sample surface damage while further etch. Reactive gas (SF_6) ions attack the sample surface while the noble gas (Ar) additive dilutes the plasma, this causes inert ion bombardment of the surface. As a consequence etch anisotropy was enhanced [151] which allowed for a deep oxide etch with highly vertical sidewall profile. The etch rate achieved during Si_3N_4 (1 µm)/SiO_2 (7 µm) etch varied with the etch window diameter and depth, but in average the etch rate for the 6 x 30 min etch was 60 nm/min. The larger the mask opening the more the reactive plasma can get into contact with the sample surface, however the deeper it gets in the opening the less reactive it is due to the residue of previously reacted components. The etch rate is highly dependent on the substrate material and its deposition method (PECVD Si_3N_4 and SiO_2 in this case) [152]. The etch depth was observed by a laser interferometer, LEP400 (intellemetrics, UK). Once the desired etch depth was achieved during the sixth run, the sample was placed in the solvent bath (not ultrasonic). First in acetone for 20 min and then in isopropanol for 5 min to release the sample from the carrier glass slide.

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Step	Description
Oxygen (O_2) ash	Gas: O_2 Gas flow rate: 10 sccm RF power: 10 W Bias voltage: 510 V Process pressure: 50 milliTorr Processing time: 10 min
Etch process: run 1	Gas: SF_6 + Ar Gas flow rate: SF_6: 30 sccm; Ar: 15 sccm RF power: 200 W Bias voltage: 510 V Process pressure: 30 milliTorr Processing time: 30 min
Inspection and measure-ment	1. Inspect the resist mask under microscope (UV blocking filter not required) for any cracks and non-uniformities that might prevent further etch process 2. Measure etch depth using surface profiler 3. If mask has correct thickness and no cracks are observed then perform further process-ing
⋮	⋮
Etch process: run 6	Gas: SF_6 + Ar Gas flow rate: SF_6: 30 sccm; Ar: 15 sccm RF power: 200 W Bias voltage: 510 V Process pressure: 30 milliTorr Processing time: 30 min
Inspection and measure-ment	1. Measure etch depth using surface profiler 2. If desired etch depth has been achieved, perform sample release and clean
Release and clean	1. Place in acetone bath for 20 min (avoid ultrasonic) 2. Place in isopropanol bath for 20 min (avoid ultrasonic) 3. Dry under gentle nitrogen blow

Table 5.2: Reactive ion etch process procedure

The second method used for the front side etch was FIB processing. The dual-beam FEI xT Nova NanoLab 200 SEM/FIB system uses a similar operation principle to a scanning electron microscope (SEM) except, rather than a narrow beam of electrons the FIB uses a focussed beam of metal ions. A liquid-metal ion source (LMIS), i.e. gallium, is placed in contact with a tungsten needle [153]. Melted gallium flows to the tip of the needle wetting its surface. At the tip of the needle the two opposing forces of surface tension and electrostatic stress form the liquid metal into a Taylor cone[29] with a diameter of ~4 nm. A large electric field exerts ionisation and a field emission of gallium ions (Ga^+) from the

[29] Cone shaped cusp observed in a hydrodynamic spray process releasing a jet of charged particles.

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tip of the tungsten needle. The metal ions are then accelerated and focussed onto a designated area on the sample by electrostatic lenses. Two modes of operation are possible; low beam currents for a sample surface imaging and high beam currents for the sample surface milling (etching), with a resolution determined by the ion beam spot size on the order of single nanometers. The source ions (Ga^+) hit the substrate surface removing the sample material, which is emitted as secondary cations or anions. Secondary electrons are produced as well. Both secondary ions and electrons can be delivered to a detector for a milling process control and imaging. Since the FIB milling doesn't require any form of a mask to be deposited on the sample surface, the front side post-processing was significantly simplified. Only an ultrasonic cleaning in an acetone bath and a rinse with isopropanol was carried out prior to the FIB milling as for the RIE (Table 5.1). No carrier glass slide was required as well since the chip was mounted onto a standard sample holder. Similarly to RIE processing the etch rate was decreasing with increasing of the etch depth. During FIB milling the sputtered particles cover an area around the opening, thus in the deeply etched aperture a residue of surface material will remain causing a decrease of the etch rate. Since there was no depth information available during FIB milling, a predicted etch depth was calculated based on the etch rate for the Si_3N_4 and SiO_2 which was 3 $\mu m^3 s^{-1}$ with an acceleration voltage of 30 kV and a beam current of 21 nA. The required etch depth therefore was exaggerated to 9 µm (instead of 8 µm). Pore sizes ranging from 10 µm x 10 µm to 16 µm x 16 µm were etched in a time of 300 s to 768 s respectively with a total milling time for all the apertures in the order of 139.2 min. The comparison between the RIE and FIB front side etched micro-pores can be seen in Figure 5.3.

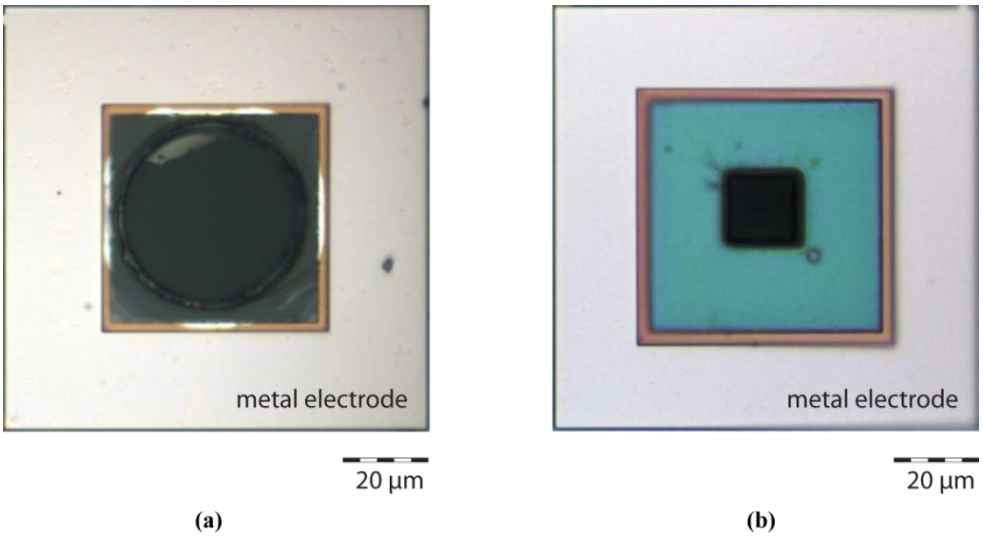

Figure 5.3: Front-side etched aperture using (a) RIE and (b) FIB process.

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While the cross-section through the FIB milled micro-pore is shown in Figure 4.24 (b).

The RIE has an advantage over the FIB processing, since all the apertures are etched simultaneously many samples can be processed (in parallel) at a time, whereas the FIB is a serial process and only one pore can be etched at a time. On the other hand the FIB process did not require any mask to be deposited on the sample, producing a more precise outcome and giving more control over the shape of the etched apertures. Once the front side processing was completed the sample was prepared for a back side etch.

5.2.2 Back-side post-processing

The back-side etch was carried out using a high aspect ratio[30] DRIE-ICP silicon etch process [154] to remove the p-type silicon substrate <100>[31] underneath the two micro-electrode arrays. The etch of the CMOS chip substrate was performed until the PMD (see Section 2.4.1) was reached, which was an etch stop layer for the back-side processing. The thickness of the silicon substrate, thus the depth of the back-side etch window, was 525 μm. The DRIE-ICP process required a photolithographically defined resist mask to expose only a desired area on the sample as for the front-side RIE. To achieve a desired etch depth a multi-layer resist mask was developed using a thick film AZ 4562 positive photoresist. The procedure for a four layer, thick film resist mask development can be seen in Table 5.3.

Step	Description
Sample, carrier microscope glass and 4''carrier wafer cleaning	1. 5 min acetone ultrasonic bath 2. 5 min methanol ultrasonic bath 3. 5 min isopropanol ultrasonic bath 3. Dry by nitrogen blow
Dehydration bake	1. Sample, carrier glass slide, and 4'' carrier wafer oven bake at 180 °C for 10 min 2. Cool down at room temperature for 10 min
Carrier glass slide coating	1. Static dispense – coat glass with AZ 4562 resist 2. Stationary – allow resist to flow for 10 s into the corners 3. Spin cycle – ramp up from 0 to 6,000 rpm at 1,000 rpm/s, hold for 10 s and ramp down from 6,000 to 0 rpm at 1,000 rpm/s
Sample attachment to the carrier glass slide	1. Attach the chip in the centre of the carrier glass slide 2. Allow resist relaxation (and solvent evaporation) at room temperature for 10 min
Soft bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 10 min 2. Cool down at room temperature for 15 min

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[30] Etch parameter defining ratio between etch depth to the mask window width.
[31] Miller index defining crystal orientation in the lattice.

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Continued from prior page	
4’’carrier wafer coating layer 1	1. Static dispense – coat wafer with AZ 4562 resist 2. Stationary – allow resist to flow for 15 s into the edge 3. Spin cycle – ramp up from 0 to 1,000 rpm at 100 rpm/s, hold for 10 s and ramp down from 1,000 to 0 rpm at 100 rpm/s 4. Allow resist relaxation (and solvent evaporation) at room temperature for 10 min
4’’carrier wafer soft bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 30 min 2. Cool down at room temperature for 15 min 3. Hold processing for 24 h to allow resist rehydration
4’’carrier wafer coating layer 2	1. Static dispense – coat wafer with AZ 4562 resist 2. Stationary – allow resist to flow for 15 s into the edge 3. Spin cycle – ramp up from 0 to 1,000 rpm at 100 rpm/s, hold for 10 s and ramp down from 1,000 to 0 rpm at 100 rpm/s 4. Allow resist relaxation (and solvent evaporation) at room temperature for 10 min
4’’carrier wafer soft bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 30 min
4’’carrier wafer hard bake	1. Oven bake in the nitrogen atmosphere at 120 °C for 30 min then, ramp the temperature down to 90 °C for 10 min 2. Cool down at room temperature for 15 min
Sample coating Deposit layer 1	1. Static dispense – coat sample with resist primer 2. Stationary – allow resist primer to flow for 5 s into the corners 3. Spin cycle – ramp up from 0 to 9,000 rpm at 1,000 rpm/s, hold for 30 s and ramp down from 9,000 to 0 rpm at 1,000 rpm/s 4. Static dispense – coat sample and glass slide with AZ 4562 resist 5. Stationary – allow resist to flow for 5 s into the corners and sample sidewalls 6. Spin cycle – ramp up from 0 to 9,000 rpm at 1,000 rpm/s, hold for 30 s and ramp down from 9,000 to 0 rpm at 1,000 rpm/s 7. Allow resist relaxation (and solvent evaporation) at room temperature for 10 min
Soft bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 30 min 2. Cool down at room temperature for 15 min 3. Hold processing for 24 h
Deposit layer 2	1. Static dispense – coat sample and glass slide with AZ 4562 resist 2. Stationary – allow resist to flow for 5 s into the corners and sample sidewalls 3. Spin cycle – ramp up from 0 to 9,000 rpm at 1,000 rpm/s, hold for 30 s and ramp down from 9,000 to 0 rpm at 1,000 rpm/s 4. Allow resist relaxation (and solvent evaporation) at room temperature for 10 min
Soft bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 30 min 2. Cool down at room temperature for 15 min 3. Hold processing for 24 h to allow resist rehydration
⋮	⋮
Deposit layer 4	1. Static dispense – coat sample and glass slide with AZ 4562 resist 2. Stationary – allow resist to flow for 5 s into the corners and sample sidewalls 3. Spin cycle – ramp up from 0 to 9,000 rpm at 1,000 rpm/s, hold for 30 s and ramp down from 9,000 to 0 rpm at 1,000 rpm/s 4. Allow resist relaxation (and solvent evaporation) at room temperature for 10 min
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Soft bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 30 min 2. Cool down at room temperature for 15 min 3. Hold processing for 2 h to allow resist rehydration
UV exposure	1. Set the mask aligner UV light source power to 7.2 mW/cm^2 2. Align the resist coated substrate with the pattern on a ferric photolithography mask using back-side alignment mode 3. Single exposure for 100 s using modes: hard and contact exposure
Post-exposure bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 10 min 2. Cool down at room temperature for 15 min 3. Hold processing for 20 min
Resist mask development	1. Prepare AZ 400 k developer in 1:4 ratio with RO water 2. Immerse sample in the solution for development for 5 min at room temperature, use continuous and gentle mixing (not ultrasonic) 3. Stop development process by placing sample in the RO water for 2 min 4. Dry by gentle nitrogen blow
Inspection and measure-ment	1. Inspect the resist film for a complete development of the mask windows (inspection need to be done under a microscope with a UV blocking filter to prevent a further expo-sure thus resist mask damage) 2. Measure mask thickness using surface profiler
Hard bake	1. Oven bake in the nitrogen atmosphere at temperature ramp up at 90 °C for 10 min to 120 °C for 30 min then ramp down at 90 °C for 10 min 2. Cool down at room temperature for 15 min
Inspection and measure-ment	1. Inspect the resist mask under microscope (UV blocking filter not required) for any cracks and non-uniformities that might prevent desirable etch process 2. Measure mask thickness using surface profiler 3. If mask has correct thickness (~ 14 µm) then it ready for the single 135 min DRIE-ICP process
Sample on the glass slide attachment onto the 4'' carrier wafer	1. Cover a small area (10 mm x 10 mm) on the 4'' carrier wafer with Cool-Grease 2. Attach the glass slide with a chip in the centre of the 4'' carrier wafer 3. Submit for DRIE-ICP process

Table 5.3: Deep reactive ion etch - inductively coupled plasma process procedure.

The process was started by a cleaning of the sample in the ultrasonic solvent bath followed by a dehydration bake at 180 °C. The sample was attached to a 22 mm x 22 mm borosilicate glass slide (back-side up) with AZ 4562 to enable easy handling while processing. The back-side coating process flow is depicted in Figure 5.4. During the test runs of etching the p-type silicon (Si) <100> substrate, the selectivity of the AZ 4562 resist mask was derived as 73:1 (the resist was etched seventy three times slower than the substrate). Therefore the resist mask needed to be over 7.2 µm thick to be able to etch as deep as 525 µm. A thick film AZ 4562 photoresist mask composed of four layers was deposited on the silicon substrate. As discussed before depositing a single layer of thick (> 10 µm) resist mask causes problems during exposure. For this reason a similar procedure as for the front-side coating

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was used, depositing a number of approximately 4.5 µm thick layers spin-coated at 9,000 rpm. Once the fourth layer of AZ 4562 resist was applied the UV exposure was performed through the photolithographic 2.5 inch ferric mask.

The photolithography mask for the back-side etch was designed as a single square opening with dimensions of 800 µm x 800 µm. The mask was also equipped with markers for the back-side alignment mode (Figure 5.5). A single UV exposure was conducted for 100 s, using a mask aligner (MA6, SUSS MicroTec) in back-side alignment mode and equipped with a UV light (400 nm wave length) source (mercury lamp), to write a mask pattern on to the positive AZ 4562 photoresist film. Once exposed the resist mask was developed in AZ 400 k developer in a 1:4 ratio with RO water solution. The development process was done at room temperature for 5 min. The process was controlled by inspecting the sample under an optical microscope equipped with a UV blocking filter. Once fully developed a measurement was performed using the surface profiler. The four layers of AZ 4562 resist developed a 14.7 µm thick resist mask. Thereafter a hard bake process was done at 120 °C for 30 min using temperature ramp up and down to prevent stress in the resist mask. After the hard bake the mask thickness was reduced to 13.7 µm, which was enough to etch through the desired 525 µm of silicon with a selectivity of 73:1. Since the DRIE-ICP machine, SPTS ICP (SPTS Technologies) required the sample to be submitted on a carrier wafer a few more steps were required. The 4 inch, 525 µm thick p-type silicon <111> carrier wafer was spin coated with two layers of AZ 4562 resist to protect it during the etch process. Once inspected and measured the sample was attached on to the wafer by using a heat conducting silver paste (COOL-GREASE, AI Technology, Inc.) [155]. The DRIE-ICP etch process was carried out for 135 min in a single run using the three-pulse recipe. However the basic three pulse recipe, also referred to as the Bosch process, was modified to use the oxygen (O_2) plasma during the depassivation pulse instead of SF_6 with Ar addition. Operation of the DRIE-ICP is similar to RIE, however in this case the chemically reactive plasma was used to remove the silicon substrate material in the resist mask window opening. After loading the sample into the processing chamber the reactive SF_6 plasma was generated in the electromagnetic field to etch the silicon. High-energy ions generated in the plasma were accelerated towards the sample surface, chemically reacting and physically sputtering the sample material (etch pulse). Subsequently the gas in the etch chamber was switched to octafluorocyclobutane (C_4F_8) for a conformal coating of the etched surface (passivation pulse). This developed a thin passivation layer of Teflon–like compound protecting the sidewalls in the etched opening against the reactive ionic species thus promoting an anisotropic etch profile. Thereafter the chamber was switched to the depassivation pulse with O_2 plasma.

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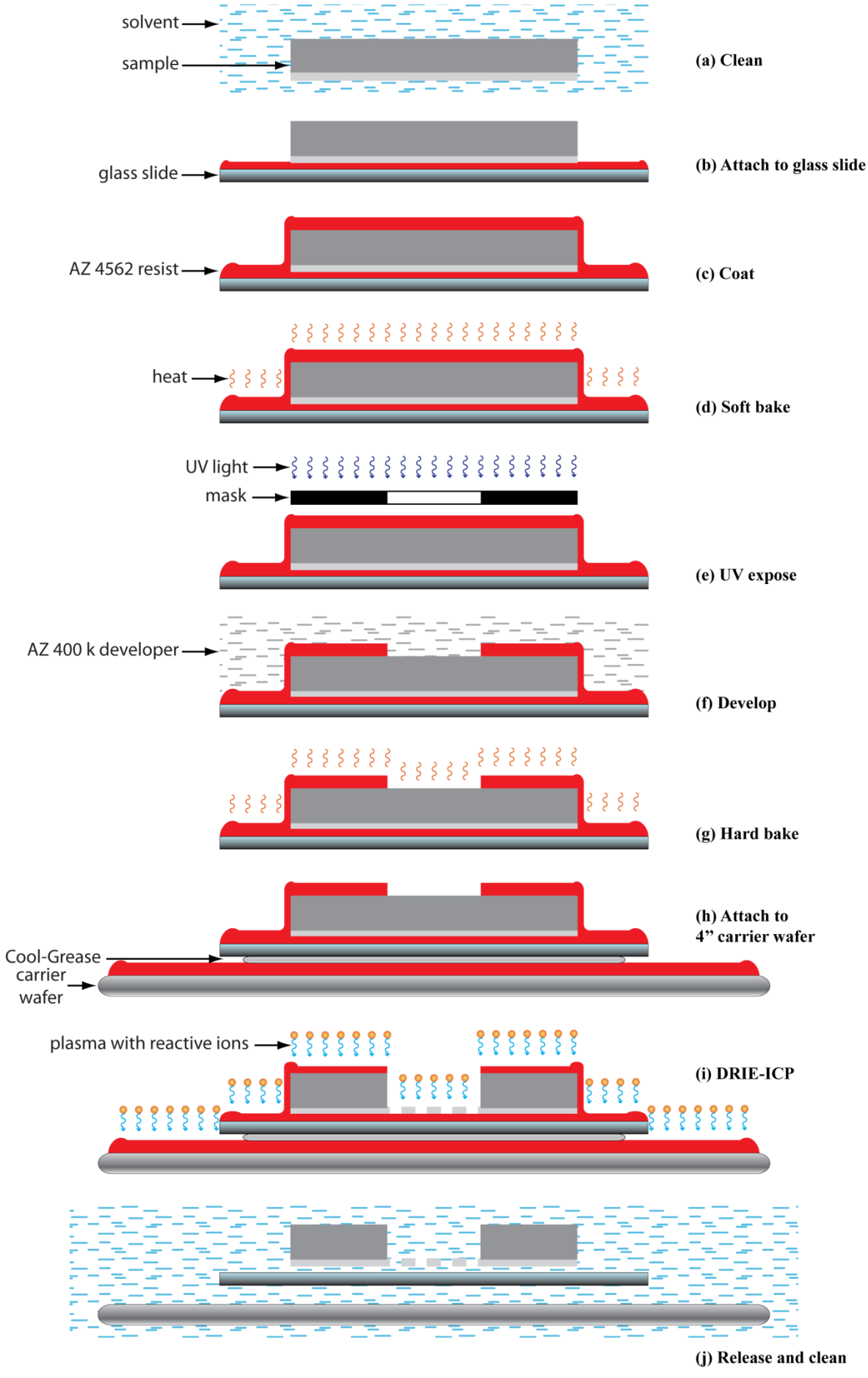

Figure 5.4: Back-side coating process flow.

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Consequently, a polymer material lining the bottom of the trench was removed exposing the silicon to the reactive plasma species for further processing in the consecutive etch pulse. Since the O_2 plasma does not chemically react with silicon, the sample substrate was etched exclusively during the etch pulse [154]. The three-pulse procedure (Table 5.4) was repeated consistently until the etch stop (PMD) layer was reached at the etch window depth of 525 µm. As the depth of the anisotropically etched aperture increased (increasing aspect-ratio), the efficient removal of the passivation layer from the base of the trench becomes more important due to a decayed ion flux which also lowers the etch rate. At a certain etch depth, dependent on the recipe parameters and the aspect-ratio, the trench may pinch off at its bottom preventing further etch process. Therefore the etch depth, thus etch rate, was controlled by a laser interferometer, LEP400 (intellemetrics, UK). The average etch rate for a 525 µm deep and 800 µm x 800 µm wide opening was 3.8 $\mu m/min^{-1}$. Once etched through, the sample together with glass slide and the carrier wafer was placed in the acetone bath for the release and cleaning process. Ultrasonic stimulation during the release and cleaning process was avoided due to a fragile (8 µm thick) on-chip membrane, instead a pipette was used to stimulate a gentle flow. The successful result of the highly anisotropic DRIE-ICP back side processing can be seen in Figure 5.6, where the top (silicon substrate) and bottom (transparent PMD layer and electrodes on Metal 1) of the aperture in visible.

Pulse	Description
Etch	Gas: SF_6 Gas flow rate: 130 sccm Coil power: 893 W Process pressure: 35 milliTorr Bias voltage: 100 V Processing time: 30 s
Passivation	Gas: C_4F_8 Gas flow rate: 110 sccm Coil power: 893 W Process pressure: 35 milliTorr Bias voltage: 0 V Processing time: 6 s
Depassivation	Gas: O_2 Gas flow rate: 13 sccm Coil power: 893 W Process pressure: 35 milliTorr Bias voltage: 100 V Processing time: 10 s

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Inspection and measure-ment	1. Since the measurement using the surface profiler is not possible at that depth, use the optical microscope to inspect back-side 2. If desired etch depth has been achieved perform sample release and clean
Release and clean	1. Place in acetone bath for 20 min (avoid ultrasonic) 2. Place in isopropanol bath for 20 min (avoid ultrasonic) 3. Dry under gentle nitrogen blow

Table 5.4: DRIE-ICP silicon processing recipe.

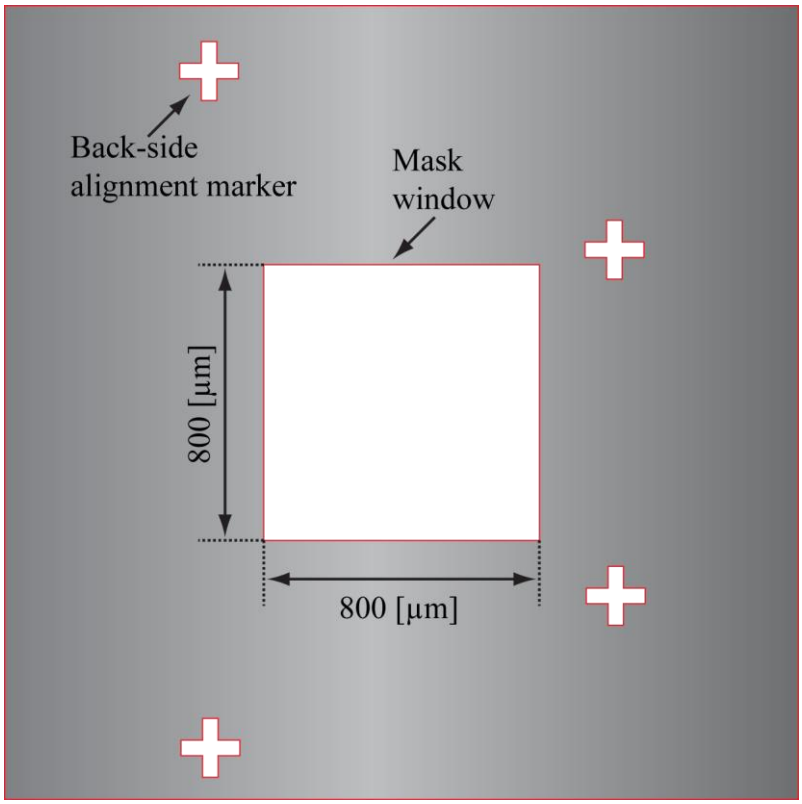

Figure 5.5: Back-side photolithography mask.

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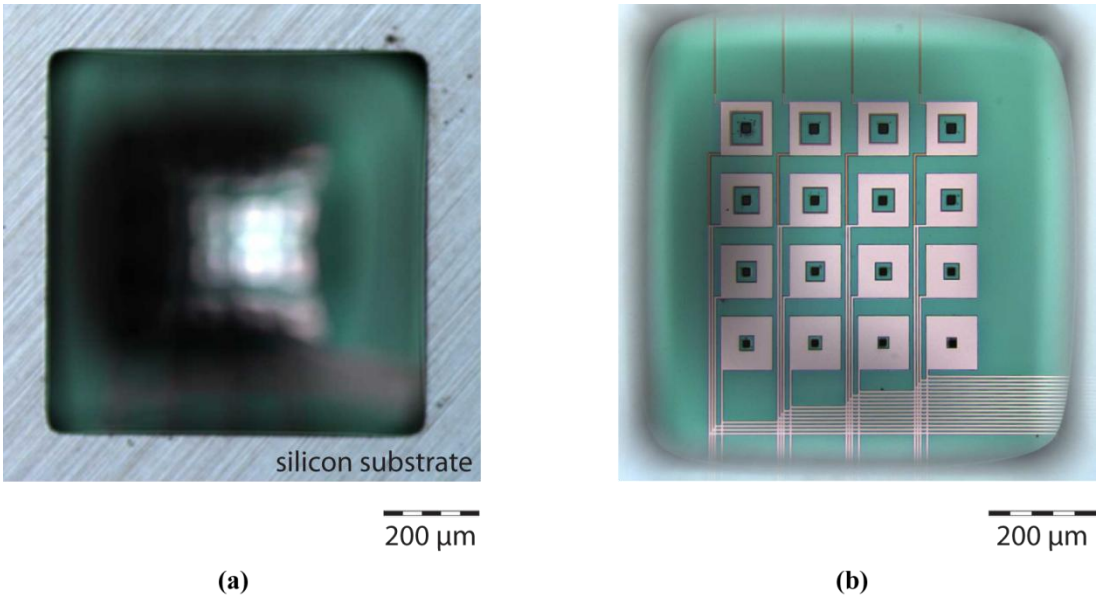

Figure 5.6: Back-side etched aperture, (a) top and (b) bottom focused view.

The DRIE-ICP is a parallel process thus a number of samples can be etched simultaneously, the space available on the 4'' carrier wafer is the limiting factor. Therefore, the simultaneous back-side etch has been done only on 4 samples while device post-processing. Etch rate and selectivity variations between the samples were negligible. At this point the on-chip membrane (Figure 5.7) with embedded micro-apertures was developed.

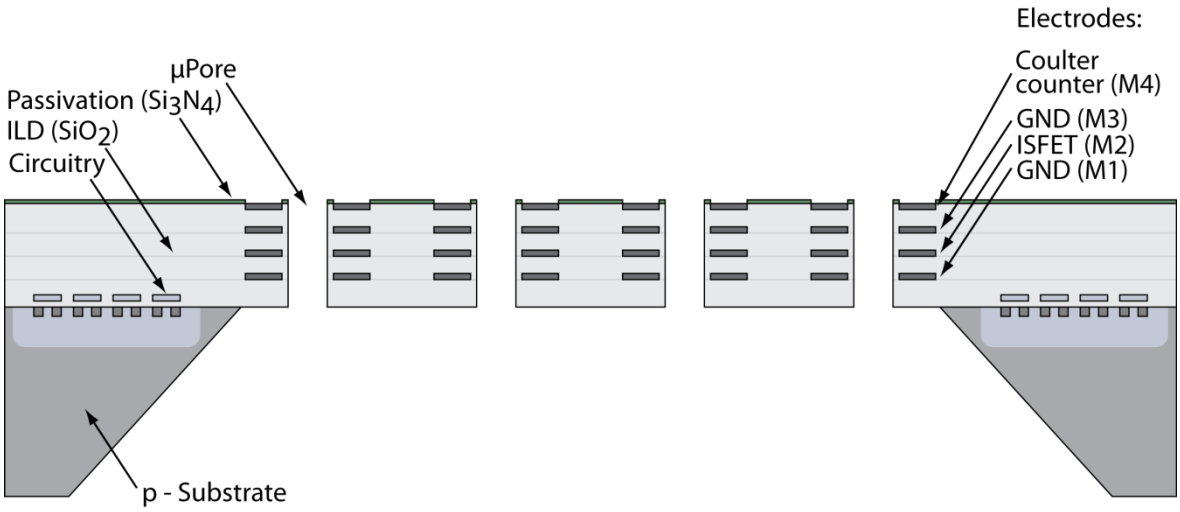

Figure 5.7: On-chip membrane with embedded sense micro-pores.

Wet etch was avoided during the post-processing due to its highly isotropic profile. The wet etch however is more selective then dry etch process [156].

Further post-processing was carried out to modify the micro-pores' interior dielectric layer which enhanced the performance of the pH sensor.

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5.2.3 Silicon nitride deposition

The silicon nitride layer was deposited inside the micro-pores utilising a process similar to the fabrication of sidewall gate's spacer for MOSFETs [157]. An inductively coupled plasma-chemical vapour deposition (ICP-CVD) process [158] was used to deposit silicon nitride, to enhance and linearise an electrochemical response of a flow-through ISFET based pH meter (see Section 2.5). To ease the small sample handling the chip was attached to a 22 mm x 22 mm borosilicate glass slide (see Section 5.2.1). The nitride deposition process was carried out at room temperature (20 °C) using a System 100 ICP 180 (Oxford instruments, UK). A custom developed two stage process was applied, which did not require any photolithography mask. As a first stage the 500 nm thick SiN film was deposited on the sample by using the conformal coating recipe given in Table 5.5. Once the sample was placed in the reaction chamber, the silane (SiH_4) and nitrogen (N_2) gases were introduced and SiN deposition was initiated in the high density plasma [159]. Thereafter, the sample was anisotropically etched to remove the lateral silicon nitride layer. Where the silicon nitride film deposited on the vertical sidewalls of micro-pores remained intact due to an anisotropic RIE profile. The RIE process was performed in a PlasmaLab System 100 (Oxford instruments, UK) using parameters given in Table 5.5. The N_2 addition to the SF_6 plasma limits the function of the active fluorine species which reduces the lateral etch rate, thus increases the process anisotropy. The etch depth was observed by a laser interferometer, LEP400 (intellemetrics, UK) by positioning the laser marker onto a top metal layer on the sample (bondpad). Once an etch depth of 500 nm was reached the process was stopped. To perform the release and clean processes, the solvent bath (without ultrasonic stimulation) was used. The SiN deposition process flow is depicted in Figure 5.8.

The developed silicon nitride layer coating the pores' sidewalls was so thin (~ 100 nm) that it could not be observed under the optical microscope or the scanning electron microscope. This is related to the fact that the sample had to be cross-sectioned (damaged) prior to the inspection and measurement. Since the number of CMOS chips was limited it was decided not to proceed with a destructive inspection and imaging. The deposited silicon nitride layer influence on the device was verified during the pH meter callibration process, this will be discussed in the following chapter.

At this point the CMOS-MEMS device was fully post-processed and ready to be tested. However to enable analyte flow through the micro-apertures embedded into the on-chip membrane, the chip had to be encapsulated. Therefore a custom microfluidic encapsulation process was developed.

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Process	Description
Carrier glass slide coating	1. Static dispense – coat glass with AZ 4562 resist 2. Stationary – allow resist to flow for 10 s into the corners 3. Spin cycle – ramp up from 0 to 6,000 rpm at 1,000 rpm/s, hold for 10 s and ramp down from 6,000 to 0 rpm at 1,000 rpm/s
Sample attachment	1. Attach the chip in the centre of the carrier glass slide 2. Allow resist relaxation (and solvent evaporation) at room temperature for 10 min
Soft bake	1. Oven bake in the nitrogen atmosphere at 90 °C for 10 min 2. Cool down at room temperature for 15 min
SiN deposition	Gas: $SiH_4 + N_2$ Gas flow rate: SiH_4: 6 sccm; N_2: 6.9 sccm Coil power: 100 W Process pressure: 4 milliTorr Processing time: 30 min
RIE process	Gas: $SF_6 + N_2$ Gas flow rate: SF_6: 10 sccm; N_2: 50 sccm RF power: 100 W Process pressure: 15 milliTorr Processing time: 30 min
Release and clean	1. Place in acetone bath for 10 min (avoid ultrasonic) 2. Place in isopropanol bath for 5 min (avoid ultrasonic) 3. Dry under gentle nitrogen blow

Table 5.5: ICP-CVD silicon nitride deposition recipe.

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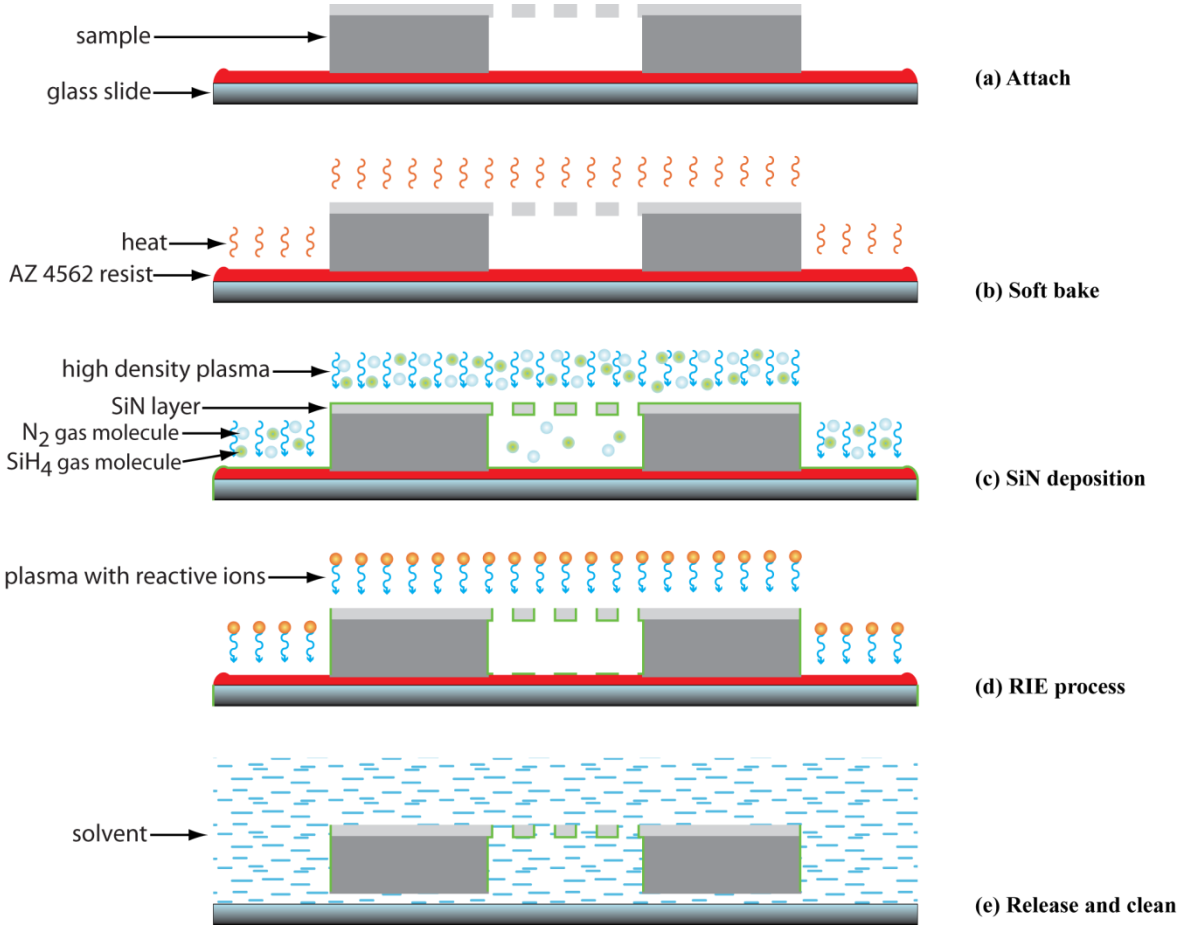

Figure 5.8: Silicon nitride deposition process flow.

5.3 Microfluidic CMOS-MEMS packaging

CMOS based microsensors usually require nonstandard packaging techniques in respect to its operation [160]. The custom develop CMOS-MEMS device utilises a flow-through methodology for its operation; where an analyte sample flows directly through the pores in the on-chip membrane. Therefore suitable encapsulation and packaging methods, compatible with an electrochemical sensor operation [161], were required.

A chip carrier was designed in the form of a 50 mm x 50 mm double-sided, flame resistant (FR4) PCB (on fiberglass substrate) using Protel (Altium Ltd). The front side of the PCB was used for signal tracks (copper) separated by screen tracks, and the back side of the PCB for the screen layer exclusively (Figure 5.9). The screen in the back was open in the centre for the back side packaging. Thereafter the PCB was milled to create a recess in its front side centre, to hold the CMOS-MEMS device in place as shown in Figure 5.10 (a). The recess has two depths, first (0.5 mm) creating an island in the centre to let the chip reside on it, and second (1 mm) to prevent the glue agglomerating in the fluidic macro-

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channel thus locking it. A macro-fluidic channel (1 mm in diameter) was also created at that stage by opening the centre of the recess.

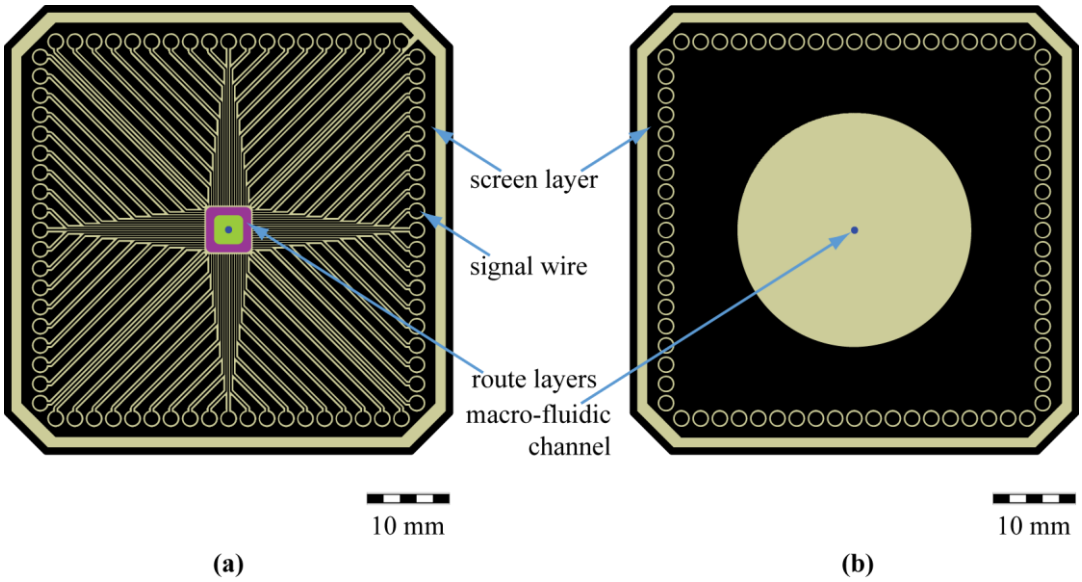

Figure 5.9: Chip carrier, (a) front and (b) back side view.

The chip was attached to the PCB using cyanoacrylate glue (Loctite 406, Henkel) as depicted in Figure 5.10 (b). Thereafter, the wire bonding process was performed by ultrasonic means using a wedge wire bonder, Bondjet 710 (Hesse & Knipps). Aluminium bond wires with a diameter of 25 µm (Figure 5.11) were used to connect the 75 on-chip pads (titanium nitride alloy) with the corresponding copper tracks on the PCB chip carrier (Figure 5.10 (c)). The macro-photograph of an actual CMOS-MEMS device wire bonded to the chip carrier can be seen in Figure 5.12. The on-chip bond-pads, bond wires and partially copper tracks were coated with the two compound epoxy adhesive (Epoxy potting compound, RS) to electrically insulate all the conducting components [162] as can be seen in Figure 5.10 (d). The epoxy encapsulant was dried for six hours at room temperature to develop a solid layer for further microfluidic encapsulation.

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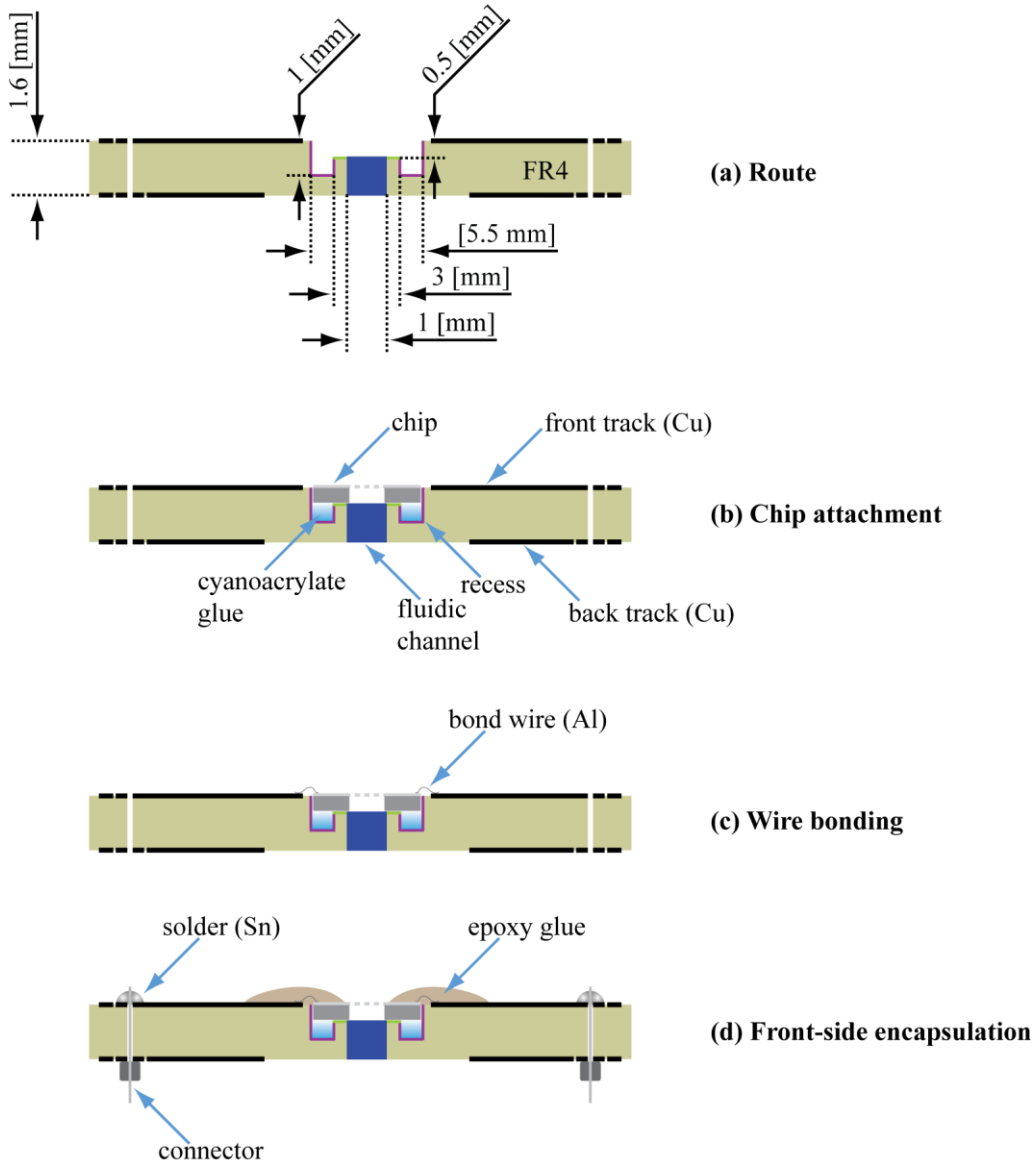

Figure 5.10: CMOS-MEMS encapsulation onto the PCB carrier – process flow diagram.

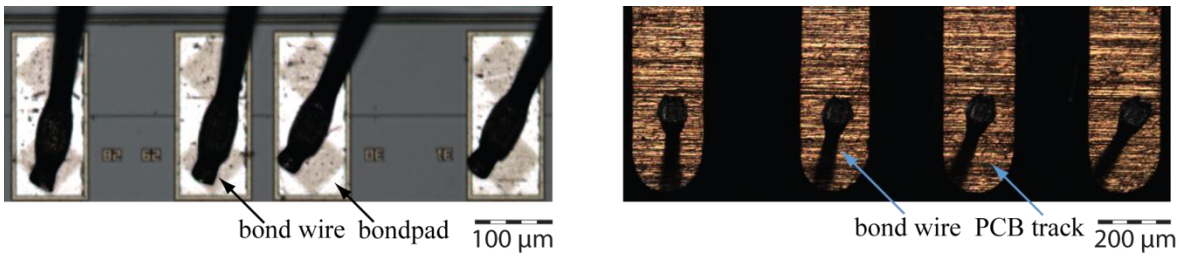

Figure 5.11: Wire bonding onto the (a) chip, (b) PCB carrier.

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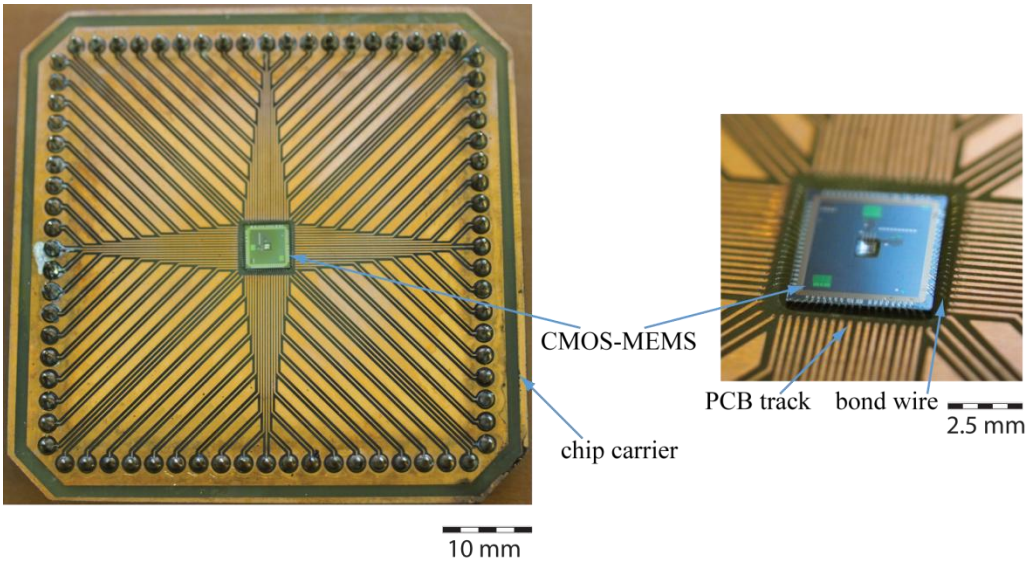

Figure 5.12: (a) CMOS-MEMS bonded to a chip carrier, (b) magnified image of the bonded device.

Chip encapsulation prevented all the conducting components except the on-chip membrane with embedded electrodes, coming into contact with the analyte solution flowing through (Figure 5.13). At this point the connectors were soldered onto the chip carrier as well. The connector layout on the chip carrier matches the one on the motherboard (not shown) enabling easy replaceability during test and measurement.

A flow-through sensors operation requires suitable encapsulation and housing methods, that perform multiple functions. The housing had to comply with a continuous analyte flow as well as being able to integrate an Ag/AgCl reference electrode in the microfluidic measurement system [163]. A microfluidic system inlet uses a polyetheretherketone (PEEK) NanoPort connector (Upchurch Scientific, Inc.), to provide connection between Teflon tubing (Upchurch Scientific, Inc.) with an inside diameter of 500 µm, and the front-side of the packaged device. The NanoPort was attached using the two compound epoxy adhesive. The back-side of the microfluidic package contains an Ag/AgCl reference electrode, RE-6 (Bioanalytical Systems, Inc.) encapsulated in a housing made of polyamide cable gland (Lapp Group), with an inside diameter on the order of 6 mm. The back-side housing was attached to the PCB using cyanoacrylate adhesive, Loctite 406 (Henkel).

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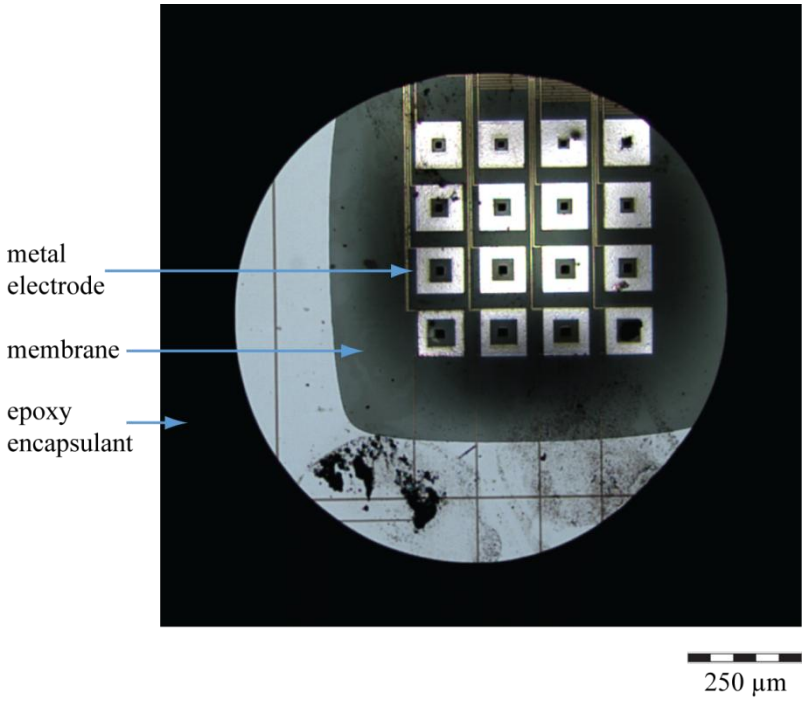

Figure 5.13: The on-chip membrane encapsulated using epoxy compound.

The microfluidic system outlet was developed from the back-side container using the PEEK NanoPort connector, to which a Teflon tubing was attached. A model image showing the front and back-side packaging methods is depicted in Figure 5.14. The analyte sample (highlighted by the dashed line) suspended in an electrolyte solution was supplied through the Teflon tubing connected to the front-side of the chip carrier. Thereafter, the analyte entered into the sense micro-pores embedded into the on-chip membrane where its parameters were measured. Once measured the sample entered the back-side container with the reference electrode from which was drained into a waste container (not shown). The microfluidic system was built with methodology enabling a continuous analyte flow through, thus long-term measurements could be taken. Any leaks in the microfluidic system, especially in the packaged module, could cause short circuits and thus an additional source of errors in the read out of the measurement system. A careful assembly with a great accuracy has been applied to prevent that. Both NanoPort connectors enable easy connectivity to the remaining part of the fluidic apparatus, as well as replaceability during the measurement system operation. The electrical connection to the reference electrode was provided through the ref. el. connector. A photograph of a packaged module of the fully operational microfluidic CMOS-MEMS device can be seen in Figure 5.15, where the front and back-side of the packaged module are shown together with the inlet and outlet tubing.

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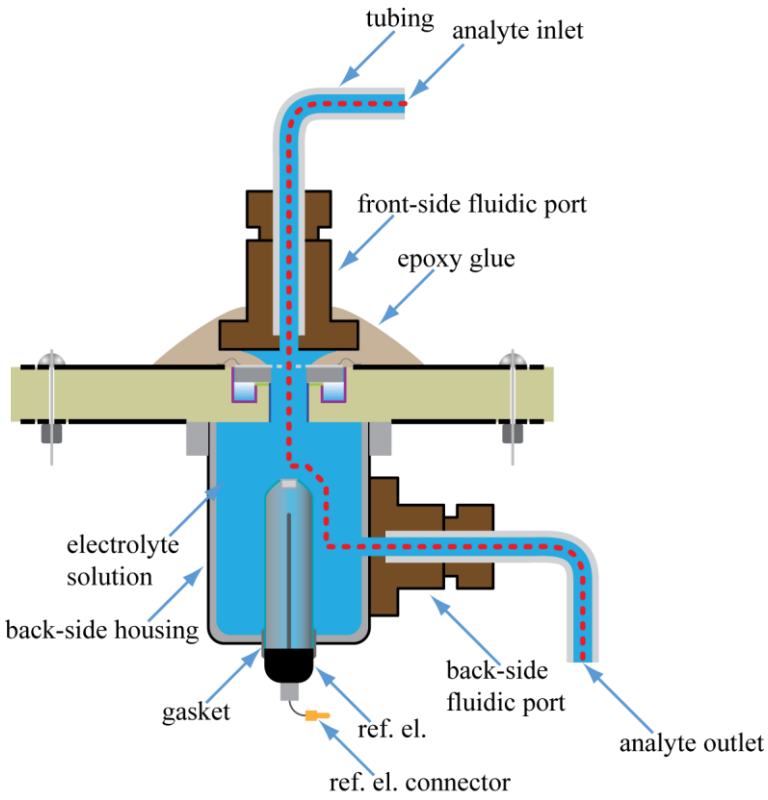

Figure 5.14: Front and back-side packaging methods.

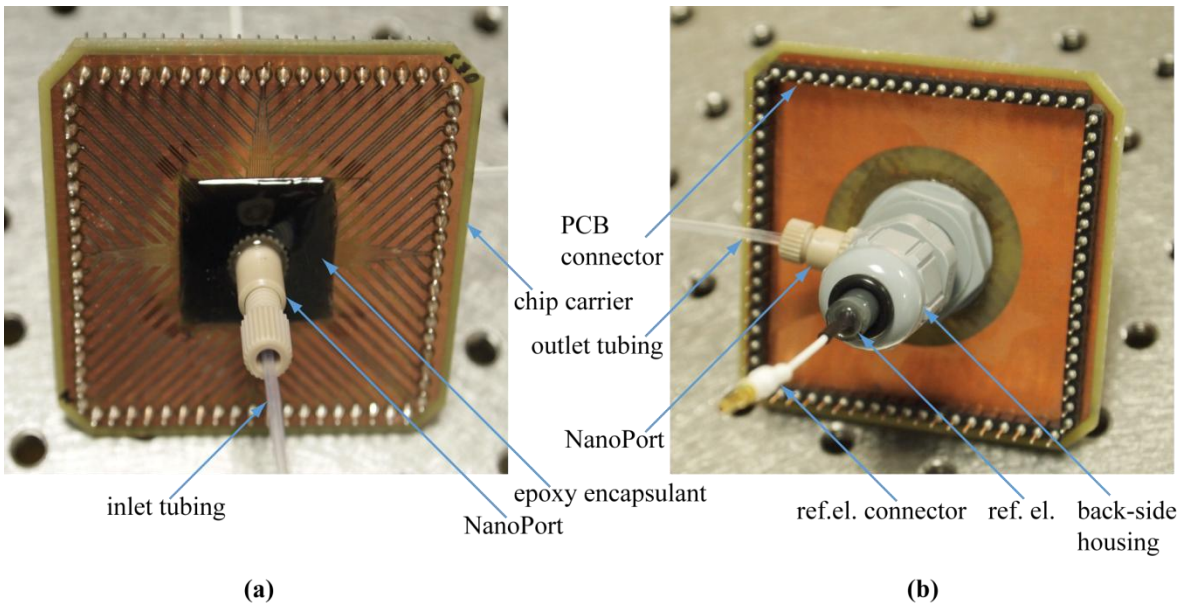

Figure 5.15: Microfluidic package (a) front and (b) back-side view.

5.4 Summary

A number of post-processing techniques have been developed to enable flow-through capability in the presented CMOS-MEMS device. The custom developed etch processes provided methods to reach a required etch depth of 9 µm in oxide and 525 µm in silicon. This

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was related to the fact that the standard processes are used at wafer level thus at the chip level these have to be modified due to a small sample i.e. sample handling and a large amount of heat generated while performing the reactive ion etch. A modification to the process was introduced in the resist mask development (multi-layer mask) procedure as well as in the etch recipe. In doing so it ensured that the front and back-side of the chip were etched through, opening the sense apertures in the on-chip membrane. Since a photo-lithographic method could not be applied for encapsulation due to a fragile on-chip membrane, a custom technique was developed to insulate all exposed (to the analyte solution) electrical connection on the chip and PCB carrier. At first the chip was positioned in the custom made recess and glued to the PCB. Thereafter, the epoxy potting compound was applied for electrical insulation. The front-side microfluidic package was attached on top using the same epoxy encapsulant. The back-side housing, together with an integrated Ag/AgCl reference electrode, was attached on the bottom of the PCB carrier using cyanoacrylate adhesive. The packaged microfluidic system was then assessed by pumping through various analyte solutions. The experimental procedures, measurement techniques and results from the developed flow-through microfluidic system are presented in the following part of this thesis.

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6 Measurement System Characterisation

6.1 Introduction

The previous chapter described the post-processing techniques used in a flow-through CMOS-MEMS development, it also enable it to be used for an electrochemical and biological experiments. In this chapter the electrochemical sensors operation is characterised; a compulsory prerequisite before any actual analyte measurement. It is important to establish sensor behaviour in operation together with the readout electronics for each of the two integrated arrays. First the experimental procedure was established enabling further experimental work. The experiments presented in this chapter were carried out using the hardware and the custom developed data acquisition software that is introduced in Section 7.

6.2 Experimental Procedure

The integrated flow-through sensor characterisation started with establishing an appropriate experimental procedure. This includes a microfluidic system inspection prior actual measurement reducing easily avoidable sources of error (electrolyte leak causes a short circuit) while in operation. Furthermore choosing instrumentation equipment with a low noise operation characteristic increases the signal to noise ratio (low noise power supplies). All these enable reliable measurement methods.

6.3 Experimental Setup

The experimental work with a flow-through sensor system requires an appropriate measurement setup to enable analyte flow through the sensing apertures (se Section 4.3.7). In order to be able to conduct experiments with a liquid analyte solution an actual microfluidic CMOS-MEMS device has to be encapsulated onto the chip carrier module and hermetically packaged (see Section 5.3). The microfluidic package was constructed with an ability to be able to integrate an Ag/AgCl reference electrode, RE-6 (Bioanalytical Systems, Inc.). Modular construction provides quick replaceability and debugging. In a typical measurement setup the CMOS-MEMS device encapsulated onto the PCB chip carrier was mounted on the motherboard using the 0.1 inch pitch Molex connectors (Figure 6.1). These two were later fitted inside the aluminium container (17.5 cm x 17.5 cm x 10 cm). The motherboard was mounted to the lid of the metal container using four 5 mm mounting screws as depicted in Figure 6.2. All electrical connections from the CMOS-MEMS device

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run to the 5 mm pitch, screw PCB terminal block (Camden Electronics Ltd.) mounted on the motherboard from which are connected to the SMA bulkhead female connectors (using copper wires with diameter of 1 mm) mounted on the lid. SMA connectors were insulated from the metal box to prevent the interference caused by ground loops (see Section 6.3.1).

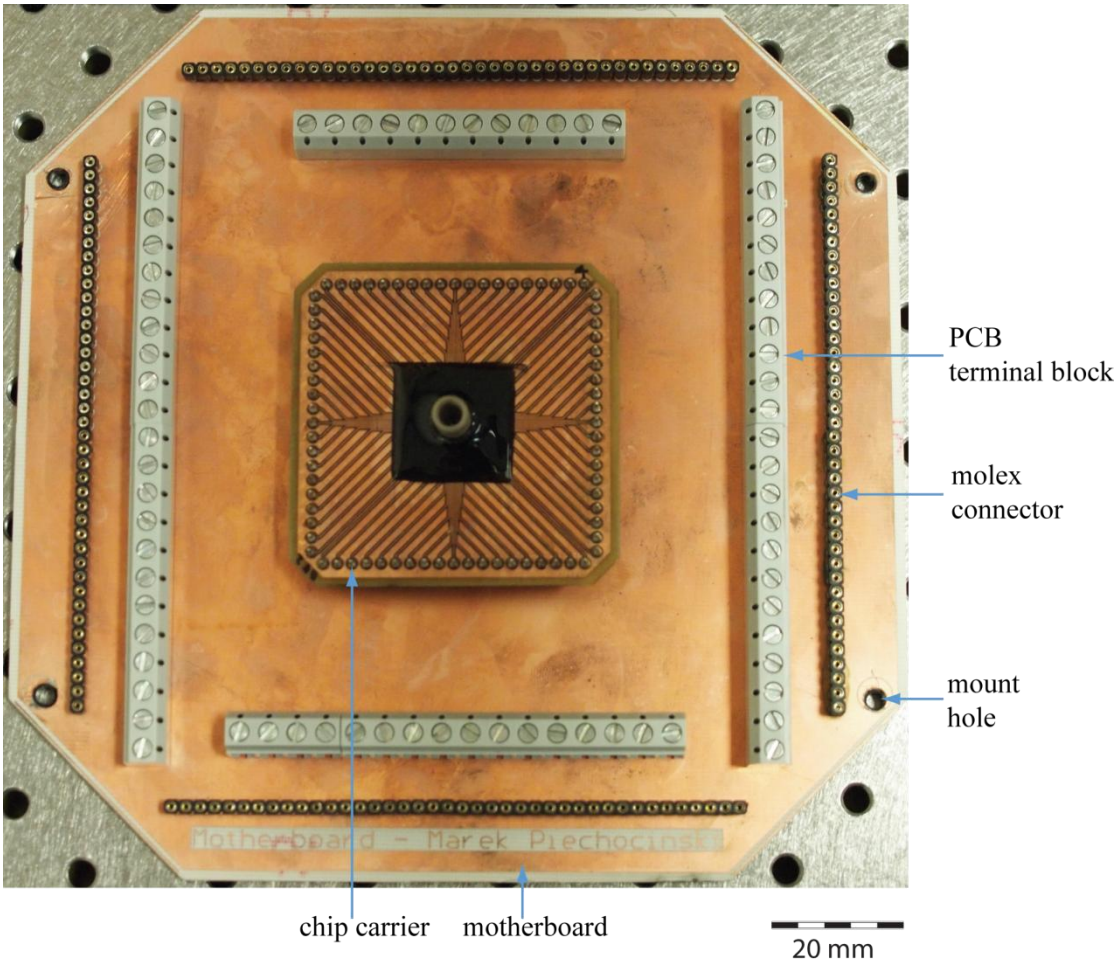

Figure 6.1: Motherboard with a mounted chip carrier.

Microfluidic inlet and outlet PEEK NanoPorts (Upchurch Scientific, Inc.) mounted on the packaged module were connected with the inlet and outlet PEEK connectors (Upchurch Scientific, Inc.) mounted on the metal enclosure using Teflon tubing with an inside diameter of 500 µm. Electrical signals to and from the sensor system were fed into to the test and measurement apparatus through the SMA to BNC coaxial cables. The analyte sample was introduced from the 20 mL syringe operated by the syringe pump, Pump 11 Pico Plus (Harvard Apparatus, Ltd.), through the microfluidic inlet PEEK connector (Upchurch Scientific, Inc.). Once measured, the analyte sample was drained into the waste container through the microfluidic outlet connector (Upchurch Scientific, Inc.). Prior to an actual measurement it was necessary to remove any air content (bubbles) from the microfluidic

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system. Therefore, the microfluidic system assembly was carried out immersed in deionised water and thereafter dried. This was related to the fact that the air content in the electrolyte solution alters its physical properties thereby the sensor electrochemical response (outputting false readout). The black epoxy encapsulant, opaque fluidic package and aluminium box acted as a barrier to the ambient light (optical radiation) which is an undesired source of noise for the ISFET operation [164] causing the threshold voltage of the ion sensor to vary [165]. The flow-through sensor system, due to its operating principle, is highly vulnerable to the interferences therefore the metal enclosure (Figure 6.3), besides its mechanical function (holding the device in place), created a Faraday cage[32] and provided screening against the electrostatic noise sources.

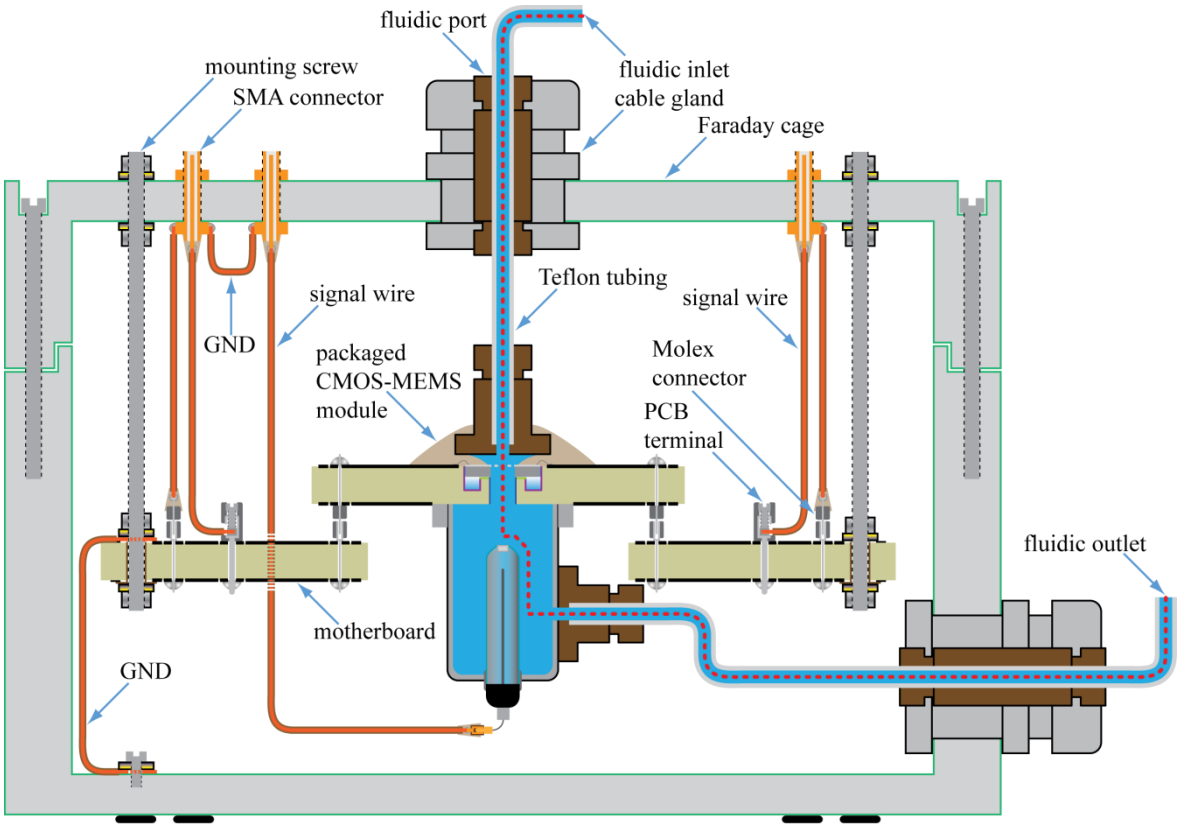

Figure 6.2: Cross-section through the microfluidic measurement system mounted inside the Faraday cage (image not to scale).

Both of the sensor arrays, in order to operate correctly, require being in contact with an electrolyte solution in which the Ag/AgCl reference electrode is immersed. Therefore, the microfluidic system had to be filled up with a liquid. The potential applied to the reference electrode depends on which sensor is used. Furthermore with the current design the simul-

[32] Enclosure made of electrically conducting material that blocks out static and non-static external electric fields.

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taneous operation of both sensors was not possible; however a solution to that problem is given in Chapter 8.

Since the sensor-system-on-chip consists of the two different sensor arrays there are two instrumentations setups for each of them. Power supply, stimulus and the bias condition are provided separately for each of the two sensors. The data acquisition and instruments control were enabled through a custom developed software (see Section 7) in LabView (National Instruments, Texas USA) graphical programming language.

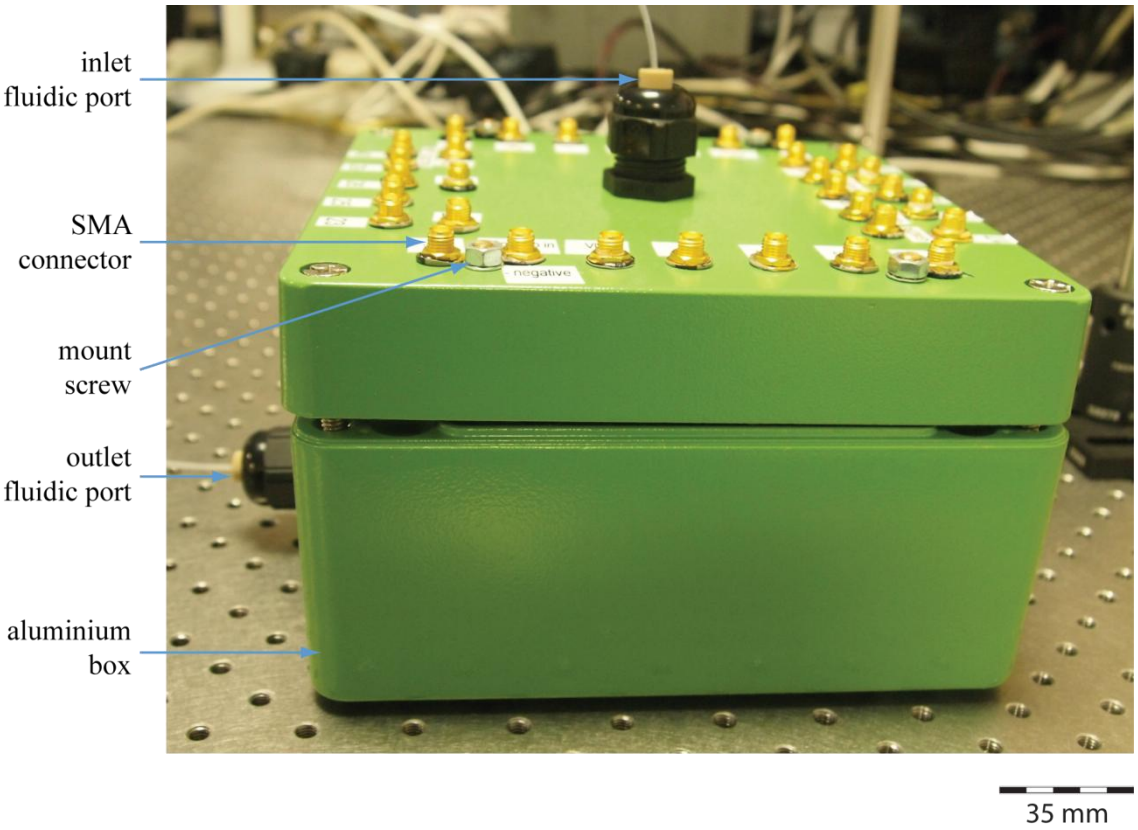

Figure 6.3: Metal enclosure (Faraday cage) with electrical and microfluidic I/O connectors.

6.3.1 Ground loops

To reduce the noise in the measurement system the signal wires were screened. Beginning on the silicon chip level, the wires between the readout circuitries, both types of sensors and input/output (I/O) bond-pads have been shielded to reduce noise coupling by capacitive and inductive means. The on-chip wire shields running above and below signal wire were connected together at a single point which was then terminated at the analogue ground bond-pad. On-chip mixed-signal circuitry has separate terminals for an analogue (GNDA) and digital ground (GNDD). These two run on to the chip carrier from which are routed on to the motherboard PCB and are connected to a common GND terminal.

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The closed circuit topology in the ground (GND) path causes the current to circulate in the closed loop. Since the physical ground circuit has non-zero impedance the voltage developed in it couples to the signal paths in the interconnects. This source of noise in the electronic circuit is termed as a ground loop [166, Chapter 5]. The ground loops were eliminated by utilising a "star" topology in a ground path as shown in Figure 6.4. Star topology in the GND circuit has be implemented at all levels in the test bench setup beginning on the CMOS-MEMS device through the chip carrier as well as the motherboard and all the way to the external instrumentation and data acquisition part of the measurement system. The screen layer on the chip carrier (Figure 5.9) and motherboard PCB (not shown) as well as the Faraday cage GND terminal are connected to the common GND terminal only at a single point to prevent closing the loop in the GND circuit in any of these. The common GND terminal is located on the motherboard PCB in the form of the 0.1 inch pitch Molex connector.

A flow-through sensor system enclosed in a Faraday cage was connected with a test bench instrumentation and data acquisition (DAQ) system using the coaxial SMA to BNC shielded cables. The screen of the coaxial cable was connected to the GND potential, however this was done only at the one end of each of the cable connectors to prevent any loops in the GND path. This was executed by insulating SMA connectors (mounted on the Faraday cage lid to which the signal wires and screen were connected) from the metal box so that the shield of a signal cable was connected directly to the common GND terminal. Isolating the SMA connector from the Faraday cage was crucial since a GND loop could be created between the common GND terminal and all of the SMA bulkhead female shield connectors shorted together.

Since the entire test bench instrumentation was powered from the single-phase AC mains the potential ground loop developed through the power network was taken into consideration. To counteract this possibility all of the test bench instruments' AC mains ground terminals except one were isolated using the appropriate multi socket extension cord so that the star topology in GND path could be maintained preventing ground loop possibility. A block diagram depicting the AC power supply from the mains for the test bench instrumentation in the measurement system with applied ground loop prevention practice is shown in Figure 6.4.

The above described methodology is known as single-point grounding [167, Section 37.6]. It improves measurement system immunity to interference caused by a changing magnetic field which induces circulating currents in a closed loop. A good example would

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be the interference caused by fluorescent[33] light sources in the measurement laboratory as well as wireless devices. For that reason it was important to power off or remove any of the wireless devices from the laboratory while carrying out the measurement experiments.

Prior to the ground loop investigation the unexpected disturbance in the Coulter counter output signal was observed as shown in Figure 6.5 (a). After an extensive investigation it was later linked to the source of a noise originating from the ground loop interference. The star topology introduced in the GND circuit successfully eliminated the erroneous signal caused by the ground loops Figure 6.5 (b).

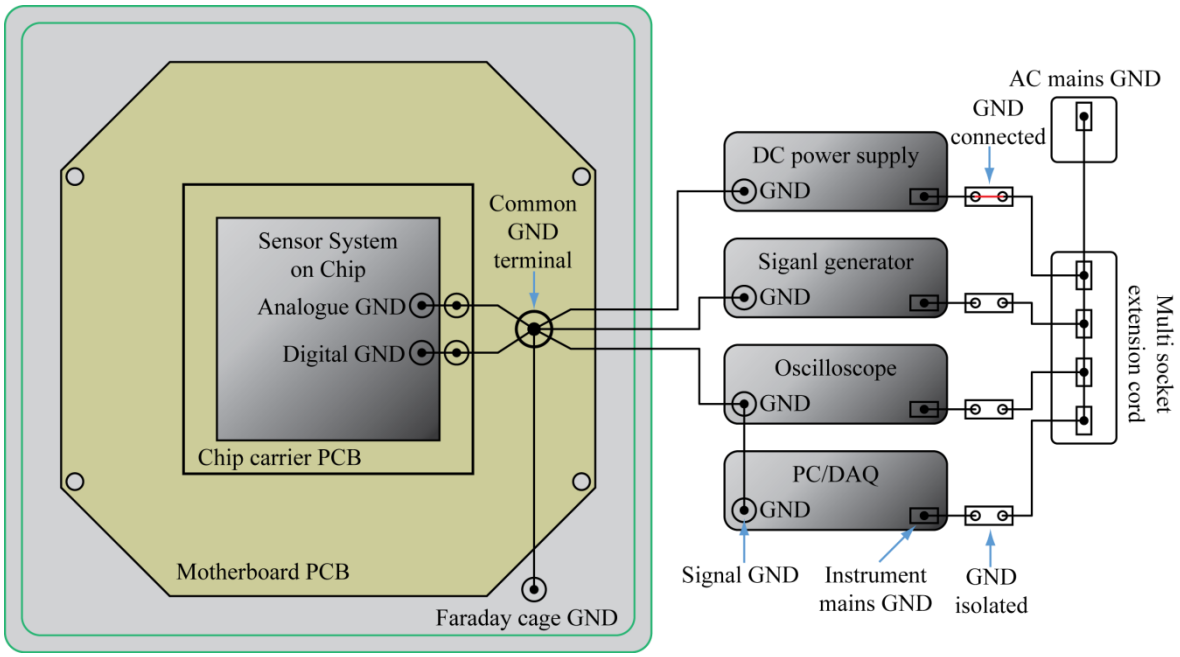

Figure 6.4: GND circuit topology in the measurement system.

Interference caused by the ground loops is not the only one that can affect the microfluidic measurement system. The interference originating from the power supply of the control instrument can be a source of noise as well. An example of which will be given in a further subsection of this chapter.

[33] Gas-discharge lamp that uses electric discharge in a mercury vapor to generate electrons which collide with phosphor exhibiting the phenomenon of luminescence (emission of light).

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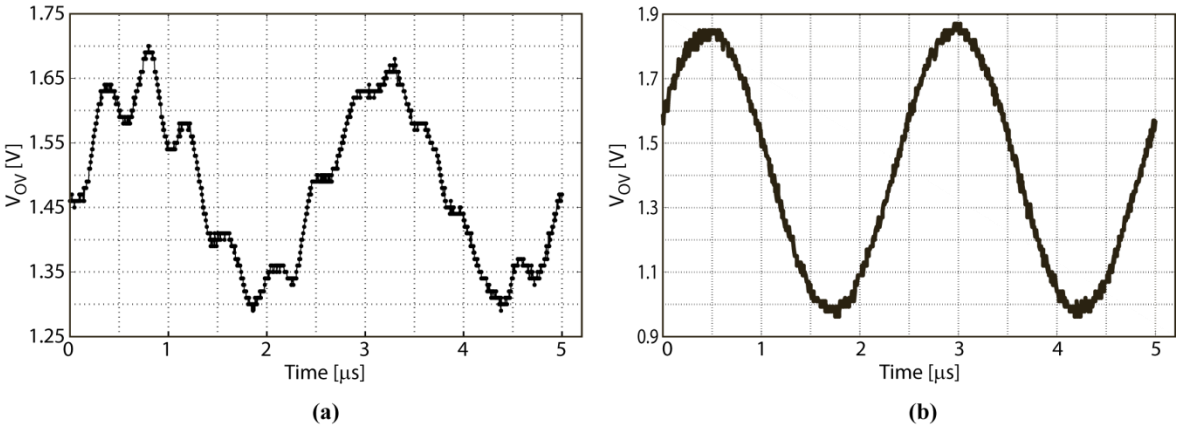

Figure 6.5: Output signal (V_{OV}) from the Coulter counter (a) with ground loops interference, (b) clean signal without interference.

6.3.2 Microfluidic system

During early experimental work the liquid analyte handling (and introducing to the system) procedure was established which helped to give an efficient measurement of living cells suspended in a buffer solution. The microfluidic system was engineered using microfluidic components as previously discussed in Section 5.3. Due to large surface tensions of the analyte solution the flow direction of a liquid had to be taken into account so that the on-chip membrane with embedded micro-pores would not be damaged. This is related to the two flow-through microfluidic containers developed during the CMOS-MEMS encapsulation and packaging process (see Section 5.3). On the front side of the module the microfluidic chamber was created between the PEEK NanoPort (Upchurch Scientific, Inc.) and the encapsulated chip (with exposed front-side of the on-chip membrane shown in Figure 5.13) while on the bottom side between the back-side of the on-chip membrane, macro-fluidic channel in the PCB, contained back-side of the chip carrier and the back-side housing (Figure 5.14 and Figure 5.15). The front side container was significantly smaller than the one in the back-side. During the experimental runs of the analyte through the system it was observed that introducing the solution from the back-side and draining it from the front-side was developing a large pressure in the back-side housing which caused leaks in the system and eventually prevented liquid going through the sensing apertures. It was later concluded that the liquid viscosity and its surface tension prevented the solution from flowing from the back-side container to the sense apertures and further to the front-side container. Enabling fluid flow in a reverse direction was an efficient way for the smooth flow-through operation. Hence the final setup utilised introduction of the analyte solution to the flow-through sensor system from the front-side (inlet) and draining it from the back-side container (outlet) as was depicted in Figure 5.14. Furthermore the small amount of liquid residing in the front-side container lowered the force exerted on the fragile on-chip

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membrane preventing its damage. This setup enabled a desired flow-through operation of the system and allowed sensor characterisation.

The speed of a liquid flowing through the system was directly related to the pressure exerted on the on-chip membrane. Therefore to minimise experiment failure due to membrane damage a number of fluid flow rates ranging from 0.5 μL/min to 15 μL/min were tested. However the membrane damage due to excessive pressure was not the only factor limiting the fluid flow rate through in the system. The goal of the experimental work was to be able to detect living cells suspended in a buffer solution therefore the flow rate needed to be set accordingly. For that reason the flow rate was set to 3 μL/min which was an optimum value to prevent on-chip membrane damage and be able to perform several experiments with various solutions within several hours of a measurement system operation.

6.4 Coulter Counter Sensor Subsystem

Characteristics for each of the two sensors were measured separately. First the flow-through Coulter counter sensor array and the readout circuitry (bridge) (see Sections 4.3.1 and 4.3.2) were characterised.

The variation in impedance of each of the sense apertures was measured between the two electrodes. An electrode pair consists of a micro-electrode embedded (on Metal 4) in each of the on-chip micro-pores (Figure 4.24) and the off-chip common (to all apertures) Ag/AgCl electrode housed in the back-side packaging container (Figure 5.14 and Figure 5.15 (b)). The impedance of the micro-pore varies with analyte properties. Therefore it depends on the electrical properties of the liquid as well as the micro-particle/cell present in the sense micro-channel (see Section 2.3 and Section 3.5). The cells suspended in the buffer solution flowing through the micro-channel modulate its impedance. This change is measured between the electrode pair.

Each of the two sensors embedded in every micro-aperture are electronically addressable. This feature was performed by analogue multiplexers (see Section 4.3.6) and a complementary decoder enabling digital logic addressing (according to Table 4.1). The analogue multiplexer was designed with a constraint of minimising its on-impedance (Z_{ON}) so that its series connection in the path with a sensor will not have a significant influence on the measured signal. However the multiplexers and the rest of the Coulter counter circuitry are physical devices residing on the same silicon substrate and are influenced by parasitic components. In order to verify the Z_{ON} of the actual multiplexer (transmission gate (TG) – its major counterpart) the Coulter counter sub-system was electronically con-

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figured. The desired TG ($S1_i$) was addressed by issuing the appropriate logical code on the decoder's inputs (*A1 – A4*) which as a result produced a "high" and "low state" on the $CSEL_i$ (index i states actual sensor number in the array) and $\overline{CSEL_i}$ terminals respectively. The remaining parts of the subsystem (op-amps, current bias circuits) were powered off (ion sensor subsystem remains powered down at all times). This enabled a single TG for the on-impedance measurement. The impedance was measured between terminals V_{S1} and E_i using the Precision Impedance Analyzer test bench instrument, Agilent 4294A (Agilent Technologies, USA). The four-terminal measurement method (see Section 3.3.1) was utilized during the experiment. Connection between the device under test (DUT) and the instrument was enabled by shielded coaxial test leads, Agilent 16048A (Agilent Technologies, USA). The shielded test leads were connected with the DUT complying with the ground loop prevention methodology (see Section 6.3.1) so that the DUT and the Impedance Analyzer's ground terminals were connected together only at a single point (not shown). Furthermore the influence of the test leads on the experiment has been compensated by calibration of the Impedance Analyzer prior to the measurement using the appropriate procedure (see Appendix C). The circuit diagram used for the multiplexer's Z_{ON} measurement is shown in Figure 6.6 (remaining part of the Coulter counter subsystem (on-chip and off-chip circuitry) is omitted for the sake of clarity). The impedance was measured for a frequency sweep ranging from 1 kHz to 1 MHz with the following stimulus conditions: oscillator voltage amplitude was set to 100 mV, frequency sweep was set to be logarithmic. The Z_{ON} was measured for all of the 16 channels. Measured Z_{ON} was in the range from 112 Ω for the channel 1 (Figure 6.7 (a)) to 110 Ω for channel 16, as can be seen in Figure 6.7 (b). For a given frequency sweep from 1 kHz to 1 MHz Z_{ON} varied by 0.5 - 2 Ω for all of the channels. Minor nonlinearity of the characteristic was observed for channel 16 which was around 300 mΩ in the amplitude between 374 kHz and 480 kHz frequency range. The discrepancy between the measured Z_{ON} of the channels was on the order of 2 % and is attributed to a manufacturing process variation and physical resistance of the interconnects. The Z_{ON} number extracted during the measurement remain within the expected value of 100 Ω with a 12 % mismatch.

Demultiplexer (*S1*) was utilised for addressing the Coulter counter therefore is connected in series with a metal micro-electrode embedded into the sense aperture. The on-chip micro-electrode makes electrical contact with an analyte solution into which the Ag/AgCl reference electrode was immersed (Figure 6.8). This electrode pair creates a capacitor whose electrical properties vary together with the impedance change of the electro-

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lyte solution in the pore. Therefore the impedance of the micro-aperture was measured (with $S1_i$ connected in series) in the next step of the calibration process.

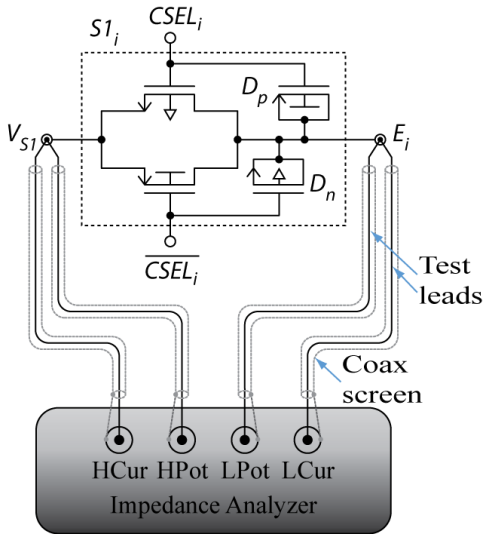

Figure 6.6: Demultiplexer's on-impedance measurement.

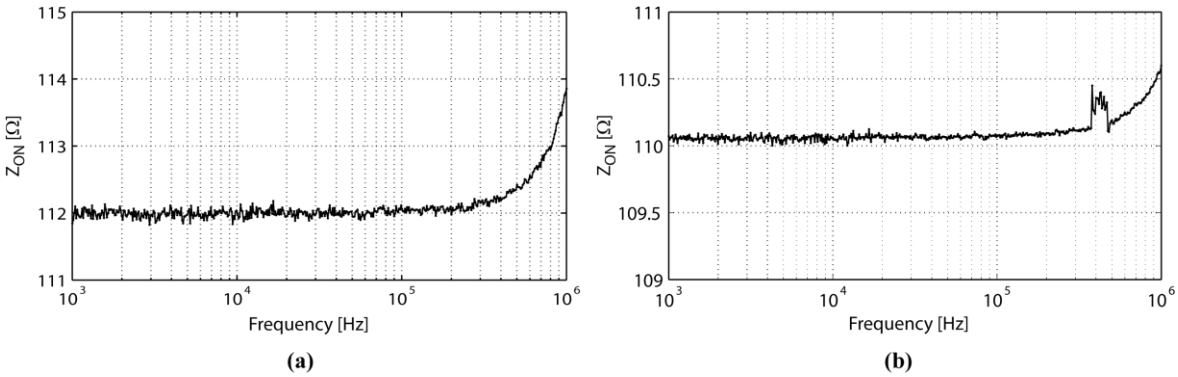

Figure 6.7: Characteristics of the on-impedance for the analogue demultiplexer (a) channel 1 and (b) channel 16.

The electrical connection was provided between the terminals V_{S1} and V_{OV} where the desired micro-pore was enabled through logically addressing appropriate terminals $CSEL_i$ and $\overline{CSEL_i}$ (Figure 6.8). The remaining parts of the Coulter counter circuit subsystem were powered off. The variation in the impedance between the sensor electrode embedded on the chip (Metal 4) and the off-chip Ag/AgCl reference electrode immersed in the liquid was measured. Coulter counter impedance ($Z_{AP\text{-}i}$) was characterised for various electrolyte solutions utilising a test and measurement setup shown in Figure 6.8. The impedance was measured (using Agilent 16048A) for frequencies ranging from 1 kHz to 1 MHz with the following stimulus conditions: oscillator voltage amplitude was set to 100 mV and a logarithmic frequency sweep. Flow-through mode of operation of the device was

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required for this measurement. Therefore, the microfluidic system developed by appropriate encapsulation and packaging methods (see Section 5.3) was put into operation (not shown).

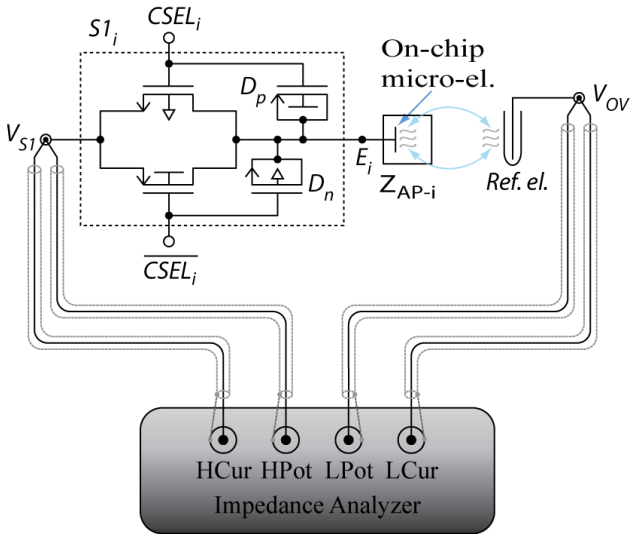

Figure 6.8: Test circuit diagram for measuring the pore's impedance.

The impedance was measured for the four micro-aperture sizes which were engineered by performing the chip postprocessing (see Section 5.2). These were 10 µm x 10 µm, 12 µm x 12 µm, 14 µm x 14 µm and 16 µm x 16 µm in size. All apertures have a depth of 8 µm which is the thickness of the on-chip membrane. The aperture impedance was measured for two different electrolyte solutions (one after another) flowing through the system with a flow rate set to 3 µL/min. Prior to the measurement a cleaning-in-place (CIP) [164] step was performed using deionised (DI) water to flush out any microscopic impurities located in the microfluidic system which may be a source of an erroneous reading. First 0.1 molar NaCl (saline) (Sigma-Aldrich Co. LLC) was flowed through the sensor system. Thereafter the mammalian cell culture medium (RPMI 1640, Life Technologies Corp.) was introduced. Between the pores' impedance measurements for the two electrolytes the CIP was carried out to remove any residue of the previously used solution. The measured impedance was the sum of the two components Z_{ON} and $Z_{AP\text{-}I}$, of which the aperture impedance was the dominant component. For the micro-pore of 10 µm x 10 µm in size with a 0.1 molar NaCl solution the impedance was ranged from 12.24 MΩ to 3.3 MΩ for a given frequency range (Figure 6.9 (a)). The impedance read for same aperture with the RPMI 1640 solution content was on the order of 5.3 MΩ - 1.56 MΩ (Figure 6.9 (b)). It was observed that the aperture impedance varied with its size much more when filled with 0.1 molar NaCl than with RPMI 1640 as shown in Figure 6.9. These results show that the sense aperture impedance is three orders of magnitude higher than the cell which is in the ~ kΩ

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range. Therefore, it will be possible to detect a significant change (decrease) in the aperture impedance due to the biological cell presence. This will be presented in Section 7.

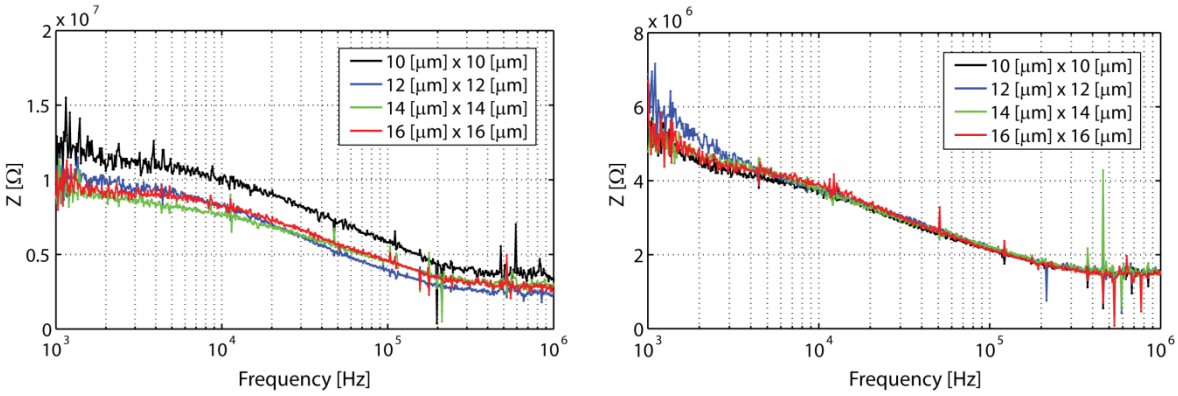

Figure 6.9: Impedance of the sense apertures containing, (a) 0.1 molar NaCl, (b) RPMI 1640. Note that colours correspond to the aperture size given in figure legend.

In the next step a bridge circuit (Figure 4.6) was characterised. This involved the test & measurement instruments to be in place to provide a power supply, stimulus, as well as a data acquisition system. A microfluidic system was operated using methodology described in Section 6.3.2. Connection between the sensor system and the test bench instrumentation was enabled by the shielded coaxial cables applying a ground loop prevention methodology (see Section 6.3.1). The measurement system was powered from a DC power supply (Agilent E3631A, Agilent Technologies, USA) (not shown) outputting 3 V and 0 V for the V_{DD} and V_{SS} levels respectively. Offset voltage, V_{OFFSET}, on the order of 1.5 V was supplied form the separate power supply. Before the Coulter counter subsystem could be operated it was necessary to determine the correct values of source, R_S, and feedback resistor, R_F (Figure 6.10) which were implemented off-chip (on motherboard PCB) since the tolerance of the on-chip polycrystalline silicon resistors is quite poor (± 20 %). This enabled flexibility in a circuit gain adjustment as well. The values chosen for R_S and R_F were on the order of 2 kΩ and 20 kΩ respectively. Therefore, the gain of the operational amplifier, $A_{op\text{-}amp}$ (Equation 4.7) was set to 10 while the gain of the instrumentation amplifier, $A_{i\text{-}amp}$ (Equation 4.3) was set during the chip design phase and was of the order of 10 as well. R_F was also used to bleed the Faradic current[34] which may saturate the op-amp A_1 (thus the bridge circuit). To be able to measure the impedance change of the selected sense aperture the Ag/AgCl reference electrode (common to all sensors) was connected to the output terminal of the A_1 as depicted in Figure 6.10. Input and output voltage values were chosen to keep V_{SIN}, V_{OI} and V_{OV} within the common mode operating range of the *i-amp* A_2 and *op-*

[34] DC current due to an input offset in op-amp A_1.

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amp A_1 respectively. Therefore the V_{SIN} supplied from the arbitrary waveform generator (Agilent 33250A, Agilent Technologies, USA) (not shown) was set to 100 mV_{PP} at 400 kHz with a 1.5 V DC offset. Without taking into account any additional parasitic components (see Section 3.3) this should produce the op-amp A_1 and i-amp A_2 output voltages V_{OV}, V_{OI} according to Equation 6.1 and Equation 4.4 respectively. Thus taking into an account the influence of the Z_{ON} and the $Z_{AP\text{-}i}$ (for RPMI 1640 solution) the expected V_{OV} amplitude was 935 mV_{PP} and 1 V_{PP} for the V_{OI} (frequency and DC offset remained the same as input).

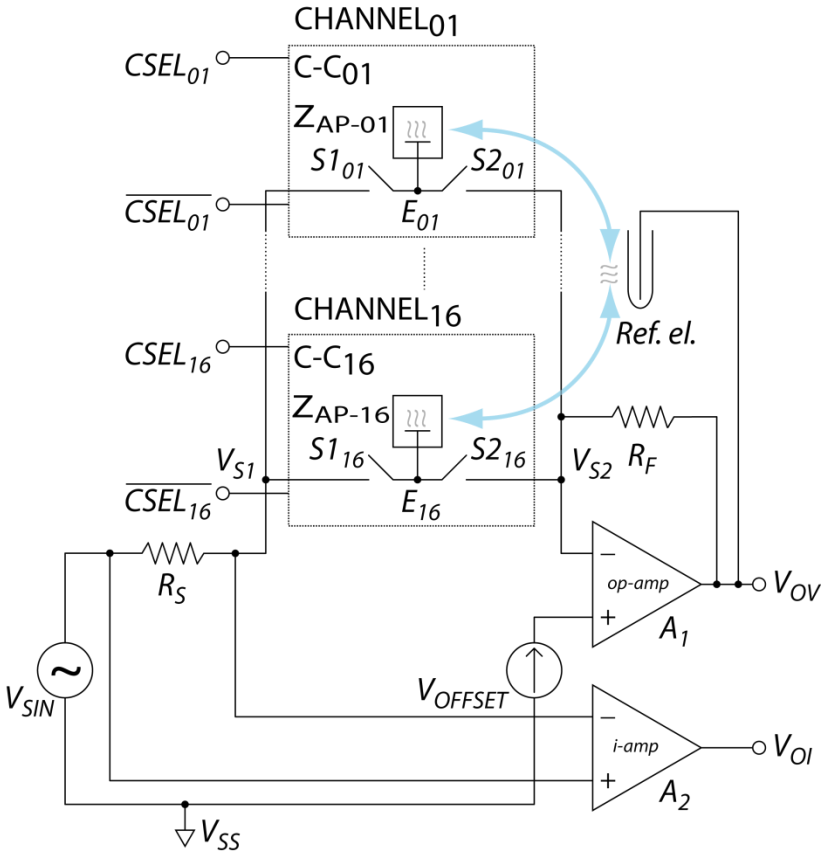

Figure 6.10: Modified Coulter counter (bridge) circuit.

$$V_{OV} = -\frac{Z_T}{R_S + Z_{ON}} V_{SIN} \tag{6.1}$$

where Z_T is the total impedance of the two components R_F and $Z_{AP\text{-}i}$ connected in parallel, $Z_{AP\text{-}i}$ is the impedance of the aperture *i* and Z_{ON} is the on-impedance of the demultiplexer *S1*. Extracting the Coulter counter impedance from $Z_{AP\text{-}i} \parallel R_F$ produces

$$Z_{AP-i} = \frac{Z_T R_F}{R_F - Z_T} \tag{6.2}$$

In the absence of any additional parasitics the single Coulter counter capacitance is

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$$C_C = \frac{1}{j\omega Z_{AP-i}} \tag{6.3}$$

Input V_{SIN} and output V_{OV}, V_{OI} signals were recorded using an oscilloscope (Agilent MSO7104A, Agilent Technologies, USA) (not shown). To perform characterisation of the readout circuitry in conjunction with the sensor structure the frequency response of the Coulter counter subsystem was measured from an input frequency spectrum of 10 kHz – 1 MHz as depicted in Figure 6.11. Since the measurement system is intended for sensing & counting red blood cells (RBC), which are 6 – 8 µm in diameter, the desired micro-pore size needs to closely match these dimensions to increase the probability of an analyte detection when present in the sense aperture (increases signal-to-noise-ratio). Hence the 10 µm x 10 µm micro-aperture size was selected for succeeding experimental work. Live biological cells require to be suspended in a cell culture medium i.e. RPMI 1640 thus further calibration of the Coulter counter circuitry has been performed with a microfluidic system containing this particular solution. From graphs depicted in Figure 6.11 it can be seen that the frequency response for both op-amp A_1 (Figure 6.11 (a)) and i-amp A_2 (Figure 6.11 (b)) is similar to the behaviour of a low pass filter [168, Chapter 1], where the output signal amplitude is significantly larger at lower frequencies than at higher frequencies. For the A_1 the output voltage amplitude for a frequency range 10 kHz – 450 kHz corresponds to an expected value, while for frequencies higher than 450 kHz it being significantly attenuated. The same behaviour was recorded for A_2, however significant attenuation of the output voltage amplitude was observed for frequencies higher than 170 kHz.

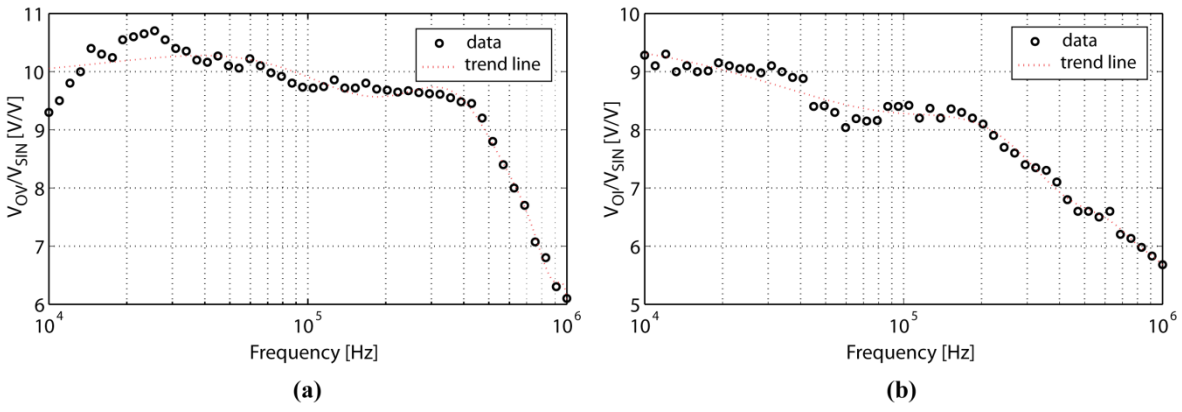

Figure 6.11: Frequency response of the (a) operational amplifier A_1 and (b) instrumentation amplifier A_2.

In the experiment, the conduction between an on-chip metal microelectrode and off-chip Ag/AgCl reference electrode is mainly capacitive due to the electrical double layer. Assuming that the capacitance of the electrical double layer (see Section 3.3) remains constant, the total reactance will be higher at lower frequencies and decreasing with

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an increase of the stimulus frequency. Hence, causing the attenuation to the signal propagating through the metal electrode-electrolyte interface. Simultaneously with the stimulus frequency increase the reactance value decreases, introducing less attenuation to the signal. Therefore, in the initial experiments the stimulus frequency was on the order of 100 kHz, but was later increased to 400 kHz so that the analyte (cell) detection probability could be maximised while operating a bridge circuit with a desired gain value.

Further calibration was carried out for the flow-through ISFET based on the ion sensor subsystem.

6.5 Ion Sensor Subsystem

The flow-through ISFET and source-and-drain followers circuitry (see Sections 4.3.3 and 4.3.4) were characterised to derive the optimum conditions to produce the highest sensitivity as well as the widest operating range.

The variation in ionic concentration of the electrolyte solution present in the sense aperture was measured by a floating gate ISFET based ion sensor. The floating gate electrode was laid out (on Metal 2) around each of the micro-pores (Figure 4.24) embedded into an on-chip membrane. The floating gate electrode is electrostatically screened by the two ground (GND) planes that run above and below on Metal 3 and Metal 1 respectively (Figure 4.24). This enables screening of the floating gate electrode from the influence of the electrolyte solution above and below the dielectric membrane. In this way the ISFET electrode is only capacitively coupled to the aqueous analyte inside the micro-pore, across the charge sensitive dielectric membrane material – silicon dioxide (SiO_2) – lining the inside of the pore (Figure 5.7). Since the ion sensor relies on an underlying MOSFET the gate terminal requires an appropriate bias voltage. This was provided by an off-chip common (to all apertures) Ag/AgCl reference electrode immersed in the electrolyte solution. The reference electrode was encapsulated in a fixed position in the back-side packaging container (Figure 5.14 and Figure 5.15 (b)) supplying the gate bias voltage V_G. Variation in the ionic concentration of the electrolyte present in the aperture modulates the surface potential of the charge sensitive dielectric membrane lining the inside of the micro-pore. This causes variation in the threshold voltage (V_T) of the ISFET which is measured. V_T however cannot be measured directly, whereas V_S can. V_S therefore is measured to observe the ISFET threshold voltage modulation due to surface charge variation. The surface charge modulation of the dielectric membrane can occur due to the change in the ionic composition of the electrolyte or by the presence in the pore of a charged particle/cell suspended in the solution.

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The flow-through ISFET sensor array is electronically addressable. This is enabled by analogue multiplexing circuitry (see Section 4.3.6) and complementary digital logic addressing (according to Table 4.1). The analogue multiplexers were designed with a constraint of minimising their on-impedance (Z_{ON}), as in the Coulter counter subsystem (see Section 6.4). The desired sensor in the array was addressed by issuing an appropriate logic code on the decoder's inputs (*D1 – D4*) which as a result produced a "high" and "low state" on the $RSEL_i$ (index i states actual sensor number in the array) and $\overline{RSEL_i}$ terminals respectively. Since the analogue multiplexer operation was verified earlier (see Section 6.4) the ion sensor subsystem calibration was initiated with characterisation of the current mirror bias circuit (see Section 4.3.5) utilising an experimental setup described in Section 6.3. An exact copy of the current source and sink circuit was layed out separately (from the main core circuitry) for testing and debugging purposes. This allows a performance assessment without the influencing the remaining parts of the ISFET subsystem. The performance of the current mirror was measured using a Semiconductor Characterisation System (Keithley 4200, Keithley Instruments Inc. USA). This instrument has several source measure units (SMUs), which can source current or supply voltage while providing simultaneous measurement of voltage or current. Three SMUs were used to extract the output characteristics of the current mirror bias circuitry. SMU1 and SMU2 were used to set or sweep the load voltage at the output terminals I-SOURCE and I-SINK respectively, while SMU3 was used to set or sweep the voltage at the V_{BIAS} terminal (Figure 6.12).

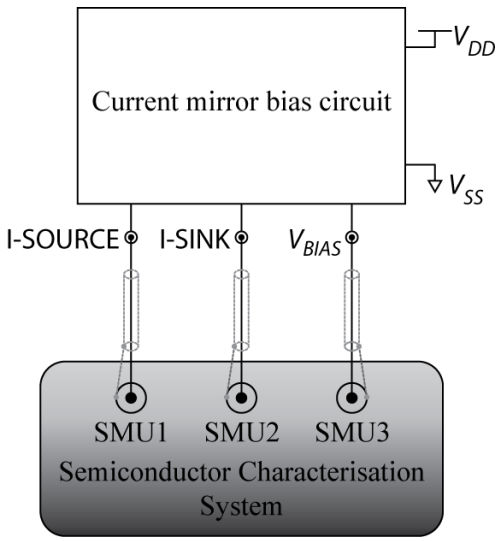

Figure 6.12: Test & measurement setup for current mirror bias circuit characterisation.

The performance of the current mirror bias circuit can be assessed on the test bench and directly compared with the simulation results outputted during the design phase (see Sec-

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tion 4.3.5). Measured results show that to output an expected 64 µA from a current source (I-SOURCE terminal) and current sink (I-SINK terminal) a potential on the order of 0.76 V at the terminal V_{BIAS} (Figure 6.13 (a)) is required. Overall performance of the current bias circuit is limited by the current source (as was observed in the simulation results in Section 4.3.5) due to its output resistance, which is lower than the output resistance of the current sink (Figure 6.13 (b)). The current source and sink drop-out voltages (for 1 % error) are comparable to the results extracted during circuit simulation. The measured output resistance, R_{out} for current source and sink were on the order of 14.1 MΩ and 45.3 MΩ respectively.

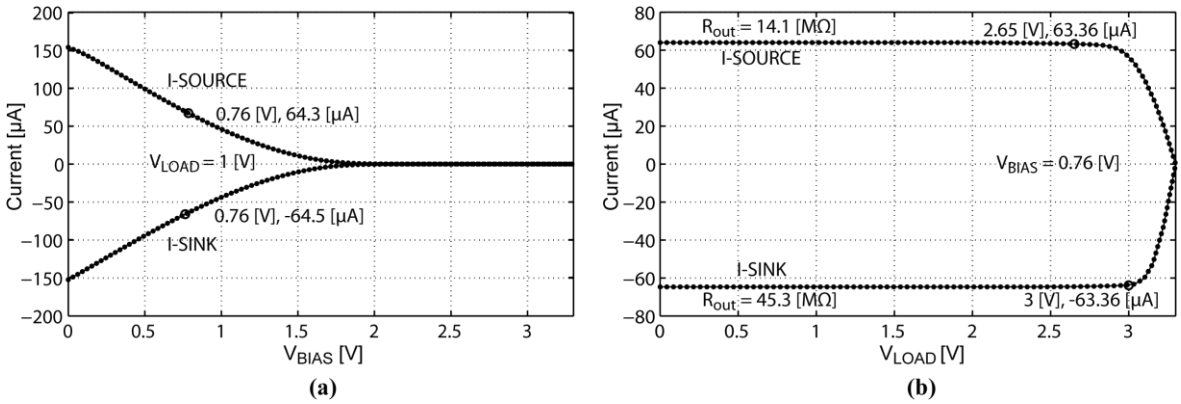

Figure 6.13: Output characteristics of the current mirror bias circuit. (a) Bias voltage sweep, (b) Output resistance.

In the next step of the test bench procedure the source-and-drain follower together with the current bias circuit, multiplexing circuitry and the flow-through ISFET sensor array were powered and put into operation to be calibrated with various aqueous solutions. The source-and-drain follower circuit uses a resistor R_{SD} with a value of 6.25 kΩ to develop a constant source-drain voltage of 400 mV (see Section 4.3.4). R_{SD} is connected off-chip (on the motherboard PCB) since the tolerance of the on-chip resistors is low. The microfluidic system setup and method of operation was kept the same as for the Coulter counter subsystem calibration (see Section 6.4). The flow rate of the aqueous solutions in the microfluidic system was kept constant and was on the order of 3 µL/min. Prior to calibration measurements with reference solutions a CIP was performed with DI water to remove any impurities and air bubbles located in the system. Furthermore the burn-in (presoak) [164, 169] process was enabled for 48 hours before any actual electrochemical measurements were taken with the device. Thereafter a joint operation of the sensor array and readout electronics was carried out to establish the linear operating range of each ISFET with a unique dielectric membrane thickness t_m (Figure 4.24 (b)). Four different aperture sizes were developed at the post-fabrication stage (see Section 5.2) thus there are

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four distinctive thickness values for the charge sensitive membrane. The ion sensor circuitry (source-and-drain follower) used in the measurement system (Figure 6.14) was powered from a DC power supply (Agilent E3631A, Agilent Technologies, USA) (not shown) outputting 3 V and 0 V for the V_{DD} and V_{SS} levels respectively. A reference electrode potential V_G was supplied from a separate power supply. The circuit configuration ensures the addressed ISFET remains in the triode regime ($V_{SD} < V_{SG} - V_T$) in which the drain current is given by

$$I_D = k'\frac{W}{L}\left(\left(V_S - V_G\right) - \left(V_T + \Delta\phi\right)\right)V_{SD} \tag{6.4}$$

The source voltage, V_S (Equation 6.5), which is the output signal from the readout circuitry (Figure 6.14) was recorded using an oscilloscope (Agilent MSO7104A, Agilent Technologies, USA) (not shown) and later acquired and stored by a DAQ system. To produce smoother characteristics the oscilloscope uses a trace averaging (with a factor of 8).

$$V_S = \frac{I_D}{k'\frac{W}{L}V_{SD}} + V_G + V_T + \Delta\phi \tag{6.5}$$

where *k'* is the process dependant constant, *W/L* is the transistor width and length ratio, V_{SD} is the source-drain voltage and $\Delta\phi$ is the electrolyte-insulator potential difference.

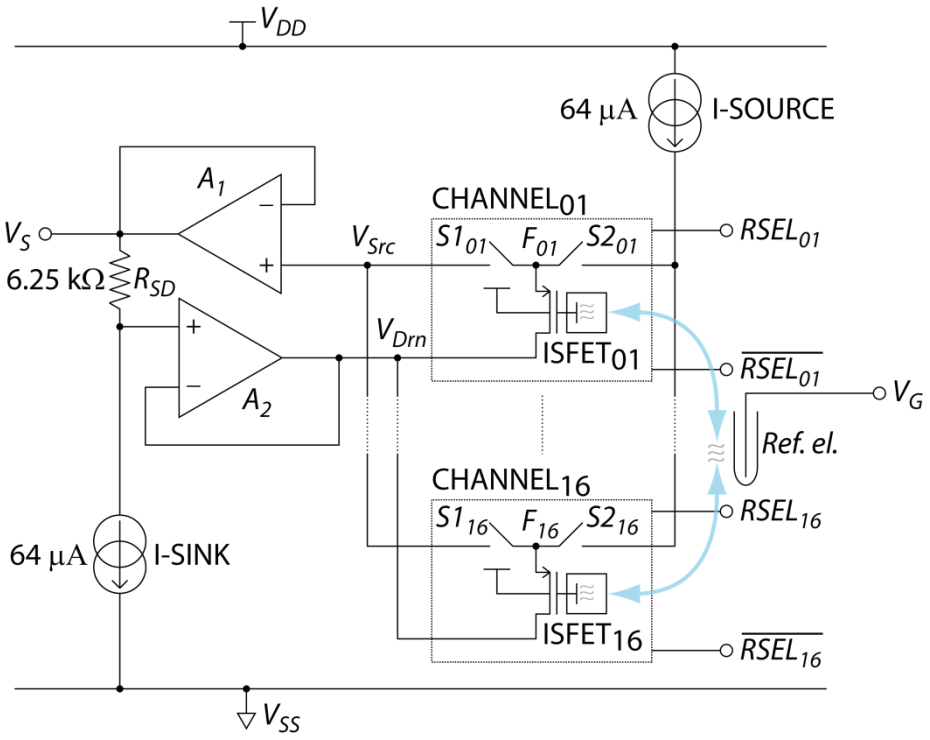

Figure 6.14: Circuit diagram for test bench measurement.

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To derive the linear operating range of the ion sensor the potential V_G was sweep across a range of values that caused the ISFET to switch on while recording the level of V_S. Measurements were performed for the solutions; 0.1 molar NaCl and RPMI 1640. SiO_2 was used as a charge sensitive dielectric membrane with a thickness determined by the micropore size. Hence, sense apertures with following t_m values, 5 µm, 9 µm, 13 µm and 17 µm were used. These values have an error of ± 2 µm due to a post-fabrication process variation. The linear range of the operating flow-through ISFET operating exposed to the 0.1 M NaCl was found to be around 1.9 V for all dielectric membrane thicknesses (Figure 6.15 (a)). Hence, considering the electrochemical sensitivity of the SiO_2 (Table 2.1) each ion sensor in the array is capable of detecting an ionic species concentration with a pH index range of 4 to 10. The same experiment was carried out for a cell culture medium, RPMI 1640, to derive the linear range of operation of the ISFET array (Figure 6.15 (b)). From Figure 6.15 it can be observed that the ion sensors behave the same for both solutions. In consequence for further experiments the reference electrode potential of -1 V was selected, since it enables a wide operating range for the ISFET based ion sensor array.

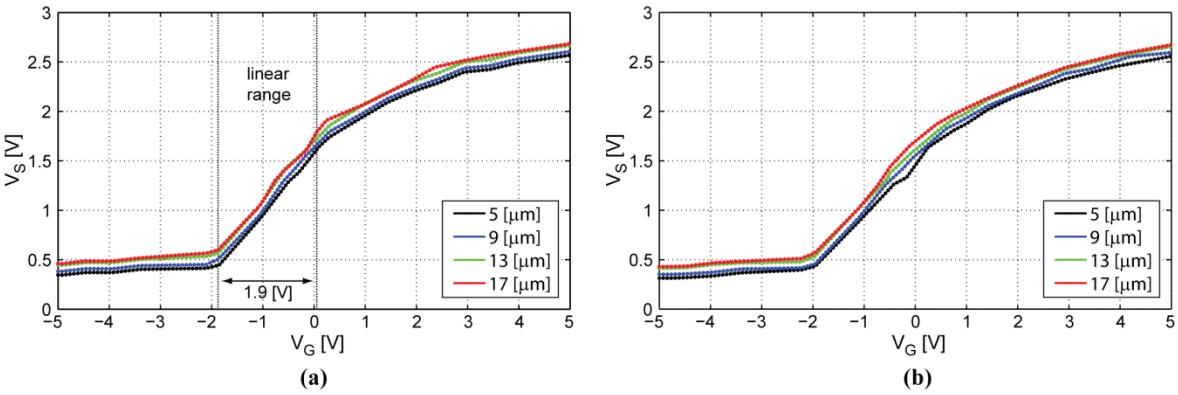

Figure 6.15: Graphs of the linear range of the ISFET exposed to (a) 0.1 M NaCl, (b) RPMI 1640. Note that colours correspond to the dielectric membrane thickness given in figure legend.

A further calibration process was carried out to assess the sensitivity of the ion sensor array. The microfluidic system was operated simultaneously with the test bench instrumentation to supply various pH reference solutions with a flow rate of 3 µL/min. The test bench setup was developed utilising methods increasing noise immunity (see Section 6.3). However this was not enough to prevent noise in the output signal. Careful assessment of noise sources in the measurement laboratory followed by a test & measurement setup tracked the source of unexpected interference down to an unreliable AC adapter of the syringe pump. The AC adapter generated a noise signal that was coupled to the measurement instrumentation through the AC mains. This problem was solved by powering the syringe pump from a

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separate low noise DC power supply. The output signal from the ion sensor subsystem with and without the noise is depicted in Figure 6.16.

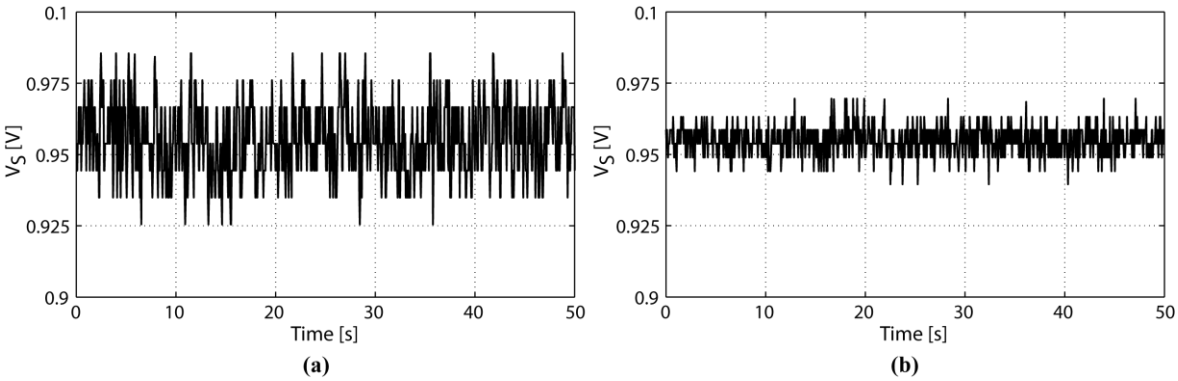

Figure 6.16: Output signal from the ion sensor subsystem. (a) With the noise generated by AC adapter of the syringe pump, (b) Noise reduced.

The amplitude of the noise introduced by the AC adapter was on the order of 30 mV. Decreasing the noise level present in the output signal allows recording the electrochemical response of the ion sensor with greater accuracy.

The pH sensitivity of the ion sensor array was measured using calibrated on-chip electronics in conjunction with a common off-chip Ag/AgCl reference electrode biased at -1 V. The flow-through ISFET is intended to be used for sensing particles/cells of diameter 6 – 8 µm. Therefore, the sense micro-pore diameter was chosen accordingly. Hence the 10 µm x 10 µm aperture size will be used for further electrochemical experiments maximising the probability of the cell detection. This aperture size determines the dielectric membrane thickness of 5 µm which should produce the largest pH sensitivity of the ISFET from all four SiO_2 membrane thicknesses used. Thus the sensitivity was assessed for a dielectric membrane thickness of 5 µm. The experiments were carried out using three distinct reference solutions with a pH index of 10, 7 and 4 (Thermo Fisher Scientific Inc.). These are flowed through the system with a constant flow rate of 3 µL/min. From the electrochemical experiment, it is observed that the flow-through ISFET array is sensitive to the ionic concentration of the solution present in the sense micro-aperture. At 29 min intervals, reference solutions are supplied to reduce the pH from 10 to an intermediate index of 7, and then to a final value of 4. Since the volume of a microfluidic system is quite large in comparison to the volume of the sense micro-pore, the time required to replace the succeeding reference solution in the system was on the order of several minutes. This caused inertia in the system.

The output signal, V_S, which was a measure of threshold voltage of the ISFET, increases with decreasing pH of the electrolyte (Figure 6.17 (a) and Figure 6.18 (a)). The

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measured electrochemical response was differentiated in terms of the charge sensitive dielectric membrane material. The sensor with a SiO_2 membrane produced a response (change in the ISFET threshold voltage, ΔV_T) of 13.3 mV/pH for the pH 4 to pH 7 index range and 53.7 mV/pH for the pH 7 to pH 10 index range (Figure 6.17 (b)). While using a Si_3N_4 membrane deposited on top of the SiO_2 produced a sensor response of 20.3 mV/pH for the pH 4 to pH 7 index range and 41 mV/pH for the pH 7 to pH 10 index range (Figure 6.18 (b)).

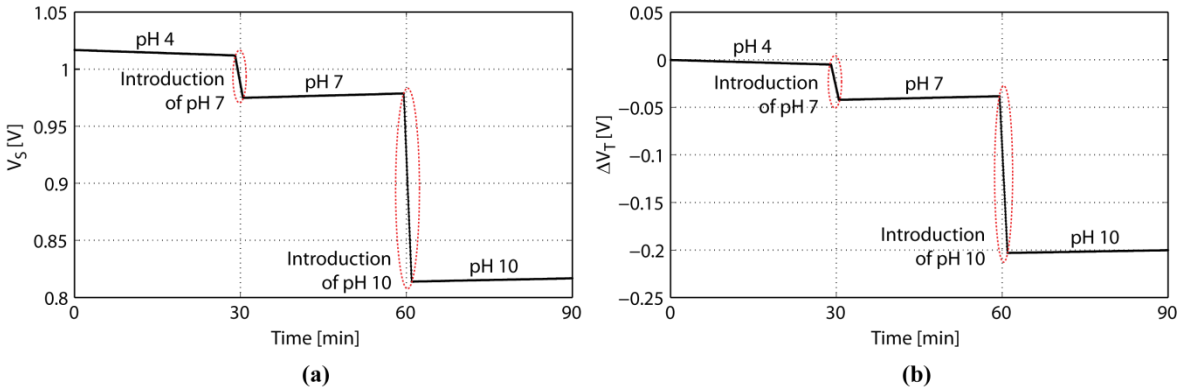

Figure 6.17: Characteristics of the electrochemical response for the ion sensor using SiO_2 membrane. (a) Source voltage, (b) Threshold voltage.

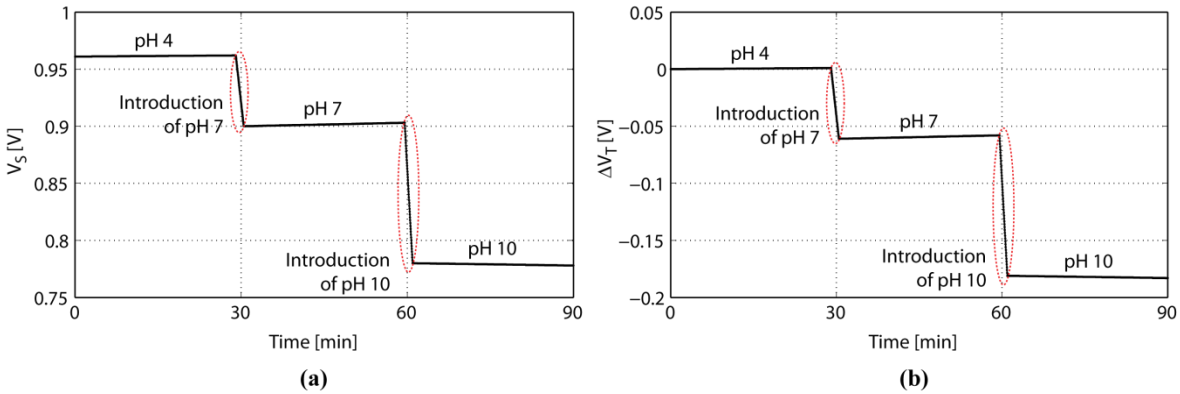

Figure 6.18: Characteristics of the electrochemical response for the ion sensor using Si_3N_4 membrane. (a) Source voltage, (b) Threshold voltage.

The calibration process allowed extraction, from Figure 6.17 (a) and Figure 6.18 (a), of the source voltage correlation with a solution's pH index for the SiO_2 (Figure 6.19 (a)) and Si_3N_4 (Figure 6.19 (b)) membrane dielectric. Altering of the dielectric membrane composition by coating the interior of the sense aperture with Si_3N_4 (see Section 5.2.3), caused the ion sensor to output a more linear electrochemical response for the proportional change in ionic concentration of the electrolyte (Figure 6.19).

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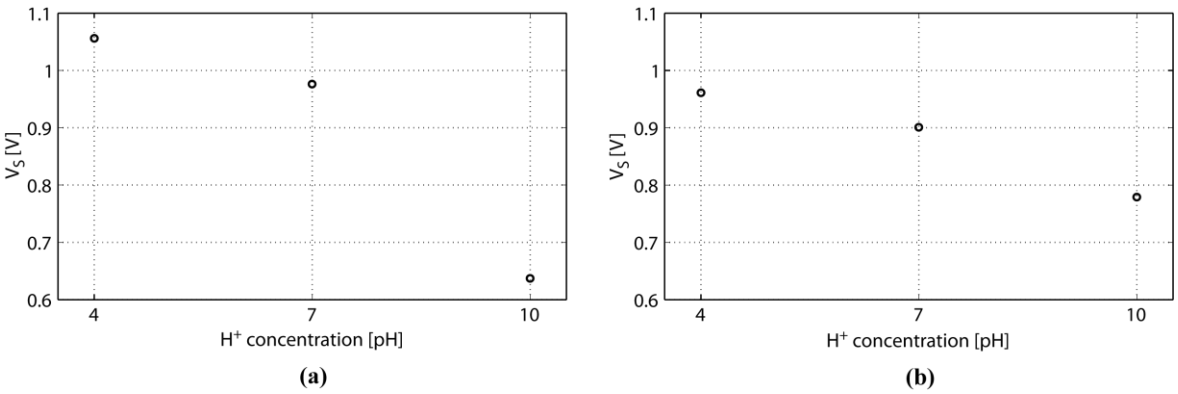

Figure 6.19: Output voltage of the sensor correlation with the hydrogen ion concentration in the aqueous solution, using (a) SiO_2 and (b) Si_3N_4 charge sensitive membrane material.

Drift [80] and hysteresis [170] which are considered as secondary effects in the ion sensor were measured as well. The drift is characterised by a relatively slow, monotonic and temporal shift in the ISFET threshold voltage, under constant temperature which is dependent on the ionic concentration in the solution. While the hysteresis (function of time constants and amplitude of slow response) of the sensor, observed with electrolyte alternation, was measured for a sequence of reference solutions introduced in the following order: pH 10 → pH 7 → pH 4→ pH 7 → pH 10. Values extracted for each of the charge sensitive membrane material can be found in Table 6.1. Devices with Si_3N_4 (deposited of top the SiO_2) membranes express lower drift and narrower hysteresis. These increase the performance of the ion sensor in terms of sensitivity and output repeatability.

Dielectric membrane material	Drift [mV/h]	Hysteresis [mV]
SiO_2	7.33	12
Si_3N_4/ SiO_2	3.33	5

Table 6.1: Drift and hysteresis values for SiO_2 and Si_3N_4 dielectric membrane material.

In this work the post-processing gave two degrees of freedom in the charge sensitive membrane development; its thickness and material composition. Considering these two variables the measured sensitivities for the dielectric membranes should vary accordingly from the theoretical values (see Section 3.3.4). Such variation was observed during electrochemical calibration. Higher sensitivity of the Si_3N_4 over the SiO_2 membrane is related to the surface groups which bind the cations or anions from the aqueous solution. The surface of the SiO_2 has a single amphoteric site while the Si_3N_4 has the two amphoteric and basic sites. This influences the linearity of the sensor characteristics as well. Therefore, the ISFET with the Si_3N_4 membrane gives a more linear response.

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6.6 Summary

After establishing of a calibration procedure for wet chemistry experiments, the two sensor subsystems were characterised separately. Readout and addressing electronics for each of the arrays were characterised and found to be able to operate in conjunction with the sensors. The Coulter counter subsystems produced good enough performance to detect the micro-pore impedance modulation caused by the presence of a biological cell. While the flow-through ISFET array, which is sensitive to the surface potential developed on the dielectric membrane, was able to detect the ionic concentration modulation within the aperture. Therefore, the charged particle suspended in the aqueous solution could be detected by measuring both the impedance and pH of the sense micro-pore. The next step will be to integrate the sensor system with the data acquisition and control software, and then use the measurement system as a flow-through cytometer for cell detection.

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7 Flow-through Cytometry System

7.1 Introduction

In this chapter, the software implementation for data acquisition and instrument control will be presented, together with an algorithm for information recovery from the acquired signal. The methods for the electrical signal acquisition involve an automated process controlled over a personal computer through the IEEE 488.2 GPIB protocol. In order to automate the measurement system, the software for instrument control, data acquisition and processing was written in the graphical programming language, LabView (National Instruments, Texas USA). Data acquired from both sensors is processed and stored on-the-fly with the measured signals being displayed on-line which gives complete control over the experimental work. The complete measurement system is then used to detect the living cells suspended in a culture medium.

7.2 Measurement Hardware

The hardware system used for stimulus, control and data acquisition from on-chip flow-through sensor arrays (see Section 4) consists of the following instruments: a personal computer (PC), a mixed signal oscilloscope (Agilent MSO7104A, Agilent Technologies, USA), a USB/GPIB controller (NI GPIB-USB-HS, National Instruments, Texas USA), a USB/RS-232 controller (USB-RS232, FTDI Ltd., UK), an arbitrary waveform generator (Agilent 33250A, Agilent Technologies, USA), three DC power supplies (Agilent E3631A, Agilent Technologies, USA), and a syringe pump (Pump 11 Pico Plus, Harvard Apparatus, Ltd.). The block diagram of the measurement setup was depicted in Figure 7.1. The automated instrumentation setup is controlled by PC (laptop) which also stores acquired data. A USB/GPIB controller allows the PC to communicate with the DC power supplies and the signal generator via the universal serial bus (USB) and general purpose interface bus (GPIB) protocols. Analyte sample supplied from the syringe pump is introduced and drained from the microfluidic system via Teflon tubing and NanoPort connectors. The syringe pump is software controlled via USB/RS232 controller. The DC power supplies establish the voltage supply rails (V_{DD} and V_{SS}) as well as the DC offset (V_{OFFSET}) required for the sensor-system-on-chip operation. The data is acquired by the PC (via USB interface) from the oscilloscope which measures the output voltages from the two sensor arrays. A PCB motherboard and Faraday cage enable a packaged CMOS-MEMS device to interface with the instruments via the Molex/PCB terminals and SMA connectors. Furthermore,

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the measurement setup was connected by shielded coaxial wires using the ground loops prevention methodology (see Section 6.3.1).

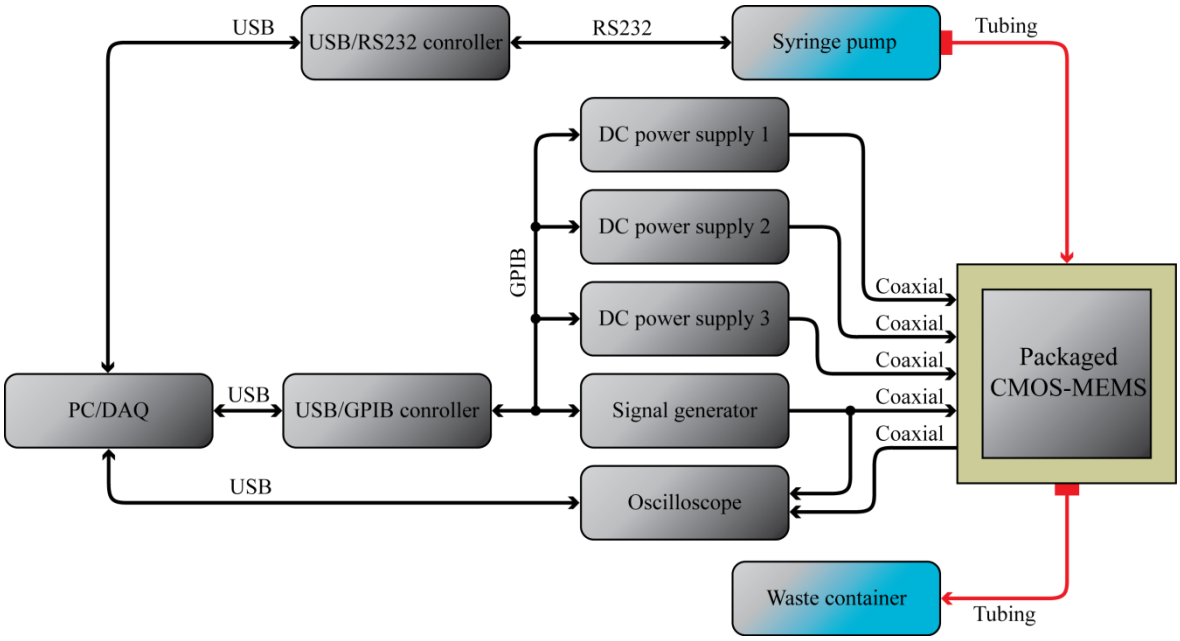

Figure 7.1: Block diagram of the measurement hardware system.

7.2.1 Data acquisition and control system

DAQ and control was coordinated from a PC by interactive software. The PC uses Microsoft Windows operating system (OS) which enables access to the standard USB ports. Three USB ports are required to perform complete DAQ and control in the measurement system. In order to communicate with the instruments, a necessary pre-requisite is to install the National Instruments I/O libraries and the graphical programing language environment on the PC. This software package includes the Virtual Instrument Software Architecture (VISA), and Measurement & Automation Explorer (MAX) utility (Figure 7.2).

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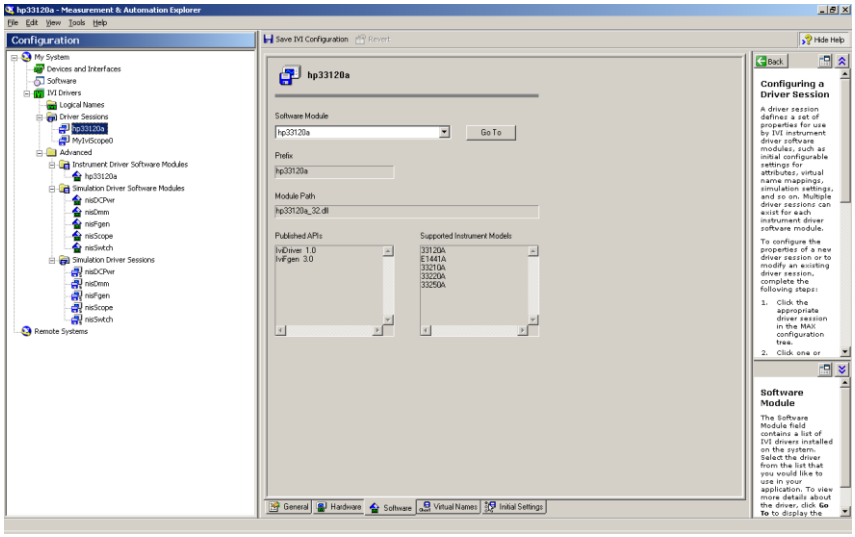

Figure 7.2: Measurement & Automation Explorer utility GUI.

In addition the drivers for each of the interfaced instruments, including USB/GPIB and USB/RS232 controllers, are required to be installed. National Instruments VISA contains I/O libraries used for the instrument drivers development. This software package allows for bidirectional communication with the hardware. NI Measurement & Automation Explorer is an I/O configuration tool with a graphical user interface (GUI) that allows the display of the installed and connected instruments. It enables management of the physical GPIB addresses of the hardware and can be used while debugging to acquire the status of the instrument via the GPIB communication protocol.

To develop a data acquisition and control application, it is necessary to install LabView graphical programming environment. Integrated development environment (IDE) is used to assemble the graphical code. The IDE is divided into two main parts, front panel (Figure 7.3) and block diagram window (Figure 7.4) which contains the actual code to be assembled. Graphical programming starts in the block diagram by putting together standard and custom library components. In the next step the GUI is arranged in the front panel view. Each window has its own live context sensitive help and debugging options accelerating DAQ software development. LabView has a unique ability to compile the code on-the-fly. Once the library blocks are placed and wired up in the block diagram window, the program is ready to be executed without further compilation.

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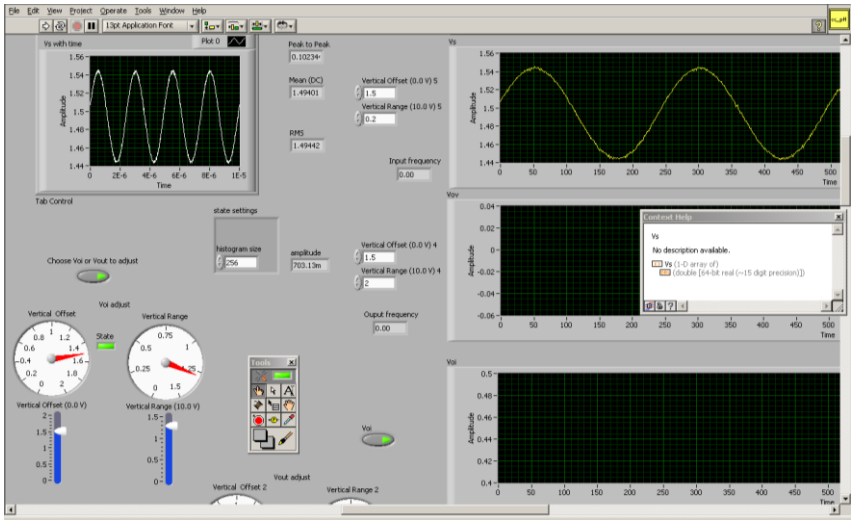

Figure 7.3: LabView IDE – front panel window.

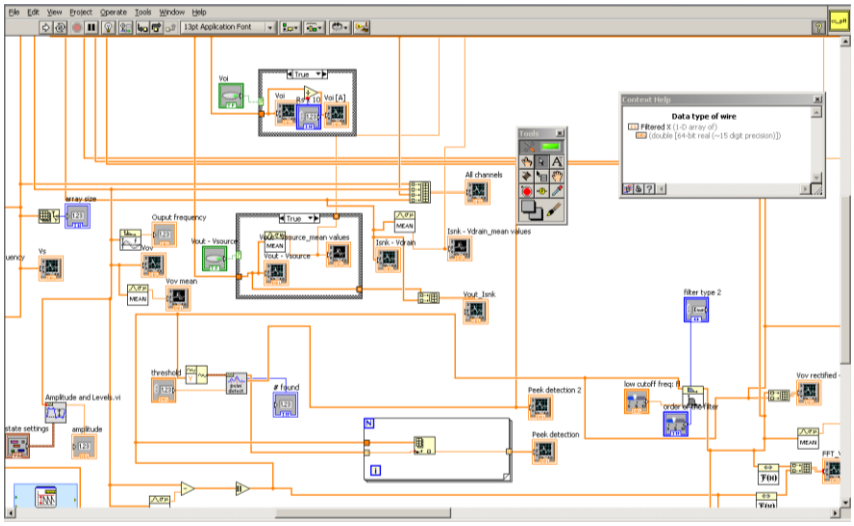

Figure 7.4: LabView IDE – block diagram window.

7.2.2 Packaged CMOS-MEMS

The encapsulated and packaged CMOS-MEMS device (see Section 5.3) is placed in a rigid aluminium box to embed it in the measurement system. The packaged silicon chip is mounted onto the motherboard PCB using Molex connectors (Figure 6.1 and Figure 6.2). All signal wires from the inside of the Faraday cage are accessible through the SMA connectors mounted on the box. Furthermore the microfluidic inlet/outlet ports are mounted on the casing to maintain the modularity of the measurement system.

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7.3 DAQ and Control Software

The source code syntax is unique for each of the GPIB accessible instruments, hence, the software is developed in a modular fashion. Each module, specific to the instrument, consists of two main components: an instrument initialisation block enabling the interface to the accessed hardware, and a function block that reads the instrument status and sends the desired set of commands enabled through the GUI. This is performed by making an appropriate call to the VISA application programming interface (API). LabView libraries specific to the hardware, and instrument drivers used to develop the DAQ and control software are provided by National Instruments.

Both controllers, the USB/RS232 and the USB/GPIB which are transparent to the DAQ and control software operate without further setup required. These two in conjunction with a USB interface allow the PC to control and acquire data from the experimental setup on a constant basis.

Instruments accessed over the GPIB protocol are organised in a star network topology, in which all of the end nodes are identified by a unique hardware address.

7.3.1 Power supply units control

In the experimental setup three power supply units are used. Two of the supplies are used to set the voltage supply rails (V_{DD} and V_{SS}), DC offset (V_{OFFSET}) and a floating gate bias (V_G). The third is used for a logical addressing of the digital inputs. Each of the DC power supplies is programmable enabling remote control over the complete function set of the device. The software uses a GUI (Figure 7.5) to control the parameters required. The DC power supply software interface module addresses the desired instrument. Once the connection is established the potential level and current limit is set for each of the voltage outputs.

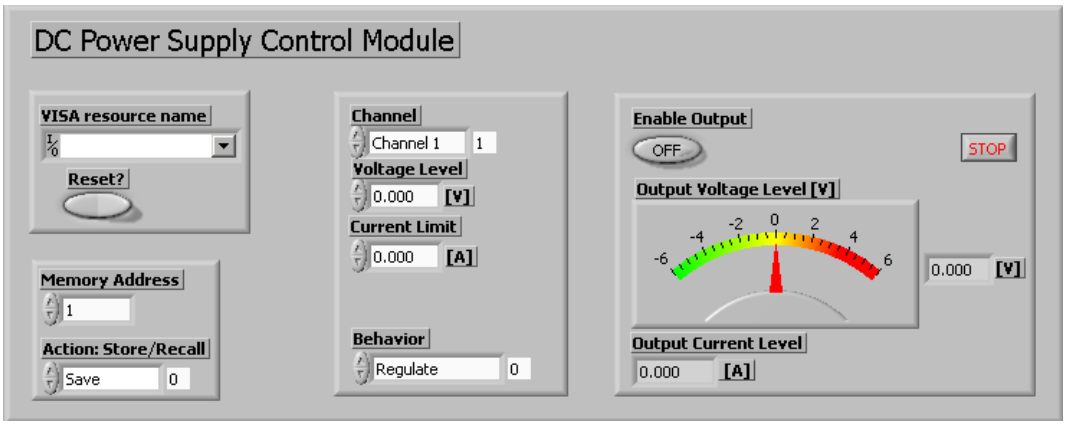

Figure 7.5: GUI of the power supply control module.

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Thereafter the output is acquired in and displayed by the voltage indicator implemented in the GUI. Finally all of the settings are stored in the instrument's memory (Figure 7.6).

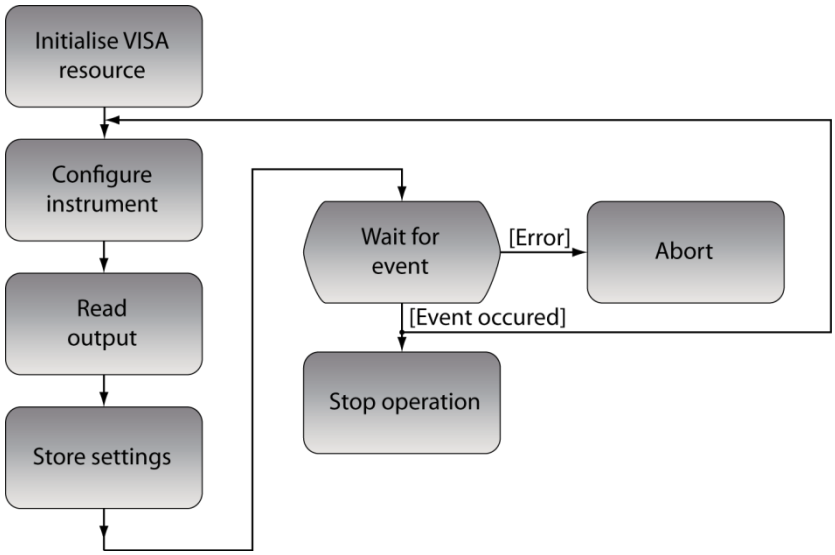

Figure 7.6: Diagram of the execution sequence of the DC power supply control software.

7.3.2 Arbitrary waveform generator control

Stimulus for the Coulter counter subsystem is supplied from the single channel arbitrary waveform generator. The instrument is programmable which allows it to be software controlled. The remote control was carried out over a GPIB communication protocol. After establishing the connection with the instrument, the software with a GUI (Figure 7.7) executes a sequence of commands to set the waveform parameters (shape, frequency, amplitude and DC offset). Communication between PC and the instrument is bidirectional. Thereafter, the output impedance of the channel and trigger level are set.

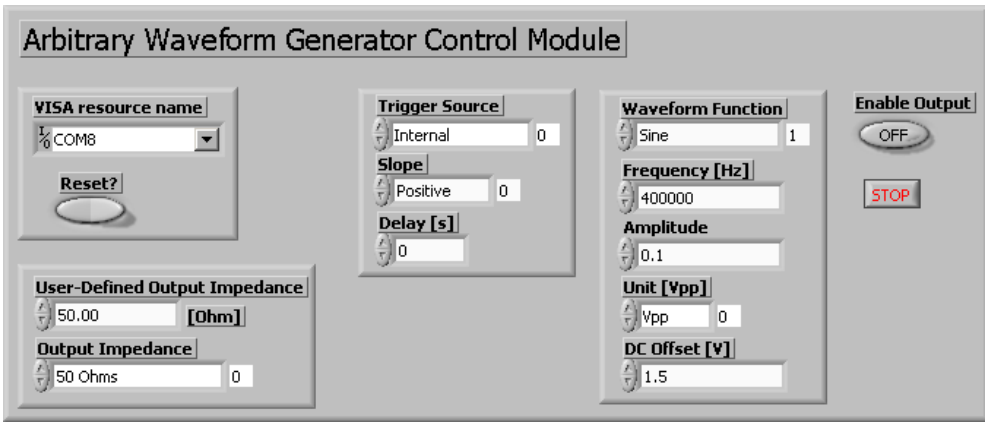

Figure 7.7 GUI of the signal generator control module.

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Finally the output of the instrument is enabled (Figure 7.8). The waveform parameters are read through the oscilloscope DAQ module interface.

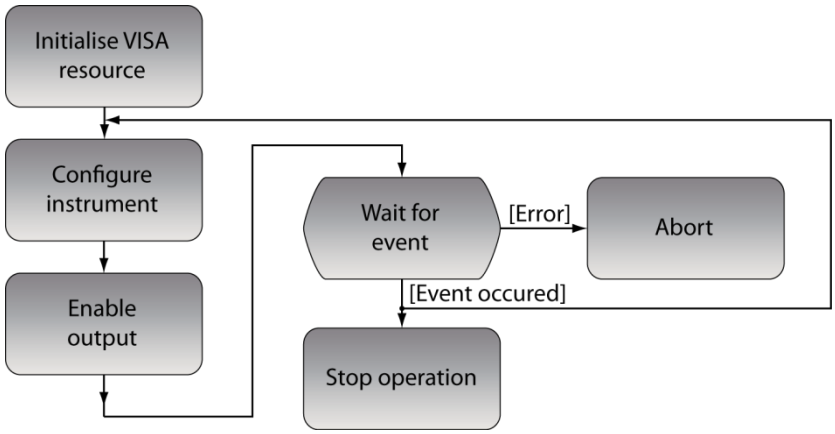

Figure 7.8: Diagram of the execution sequence of the waveform generator control software.

7.3.3 Syringe pump control

The measurement system uses a microfluidic flow-through subsystem to introduce and drain an analyte sample. The sample suspended in aqueous solution is supplied from a syringe mounted onto a software controlled pump. Developed software uses a GUI (Figure 7.9) to remotely set the desired syringe pump parameters. The syringe pump is accessed over RS232 communication protocol. The software control module establishes the connection to perform a bidirectional communication with the instrument. Thereafter, the sequence of commands is executed to configure the pump (Figure 7.10). Further configuration encompasses setting up the direction of the syringe piston movement (infuse/withdrawn) and a fluid flow rate.

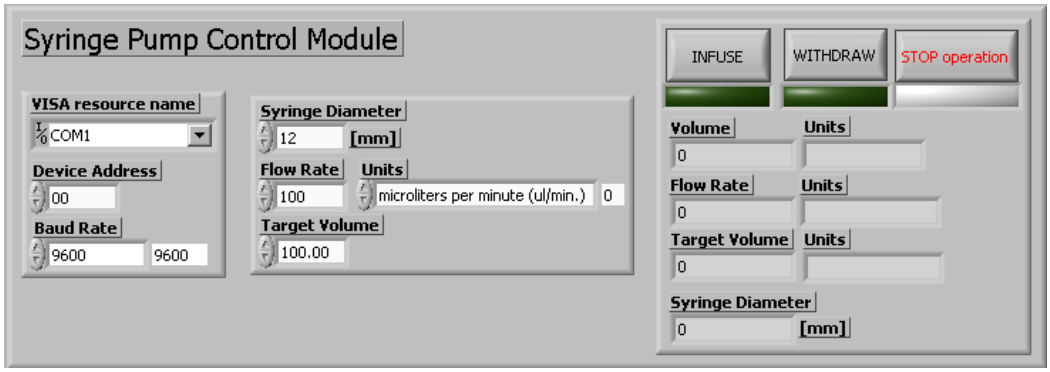

Figure 7.9: GUI of the syringe pump control module.

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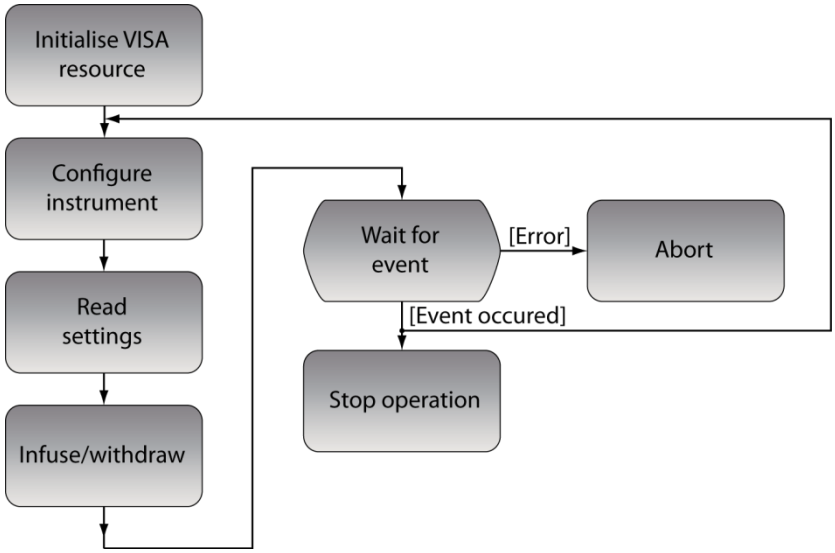

Figure 7.10: Diagram of the execution sequence of the syringe pump control software.

7.3.4 Oscilloscope control

A mixed signal oscilloscope operating in a real-time mode allows the recording of the output voltages from the sensor system. The analogue signals are fed into four separate channels. Each channel operates within a discrete voltage range, but the time base is common to all. Remote control of the instrument and DAQ is carried out over the USB communication protocol. Software uses GUI (Figure 7.11) to allow the user to configure specific functions of the oscilloscope.

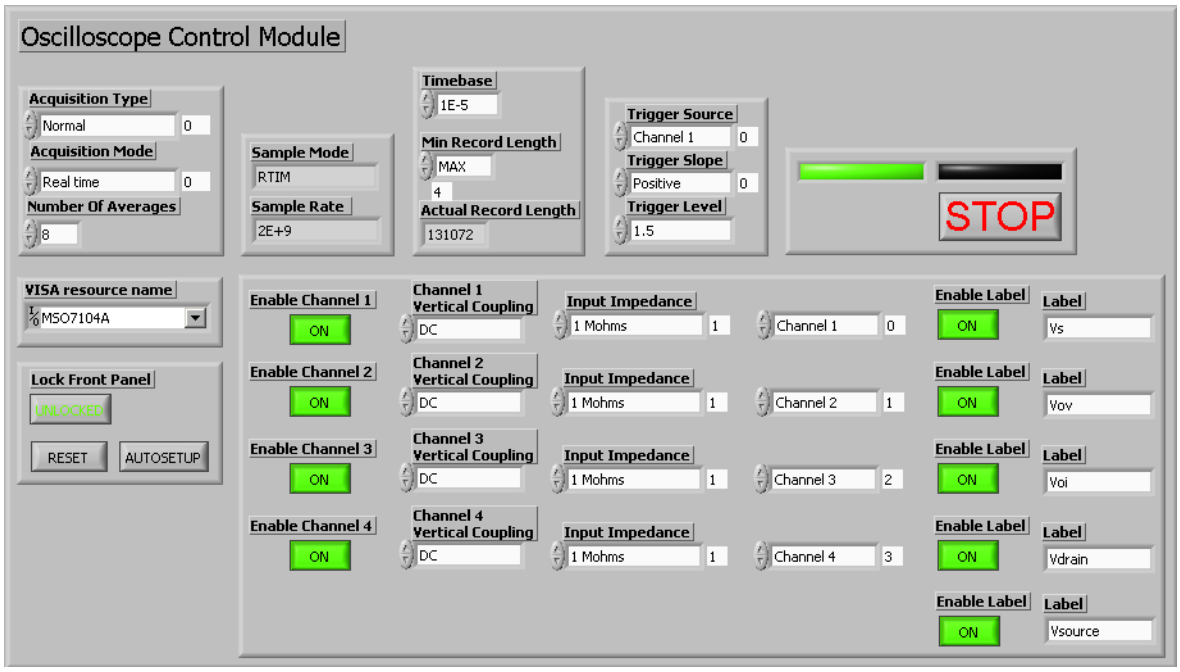

Figure 7.11: GUI of the oscilloscope control module.

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A sequence of commands (Figure 7.12) sent to the instrument enables desired channels, sets time base, voltage ranges (adjusted through a DAQ module GUI), DC offset, coupling, input impedance, mode of operation and trigger source.

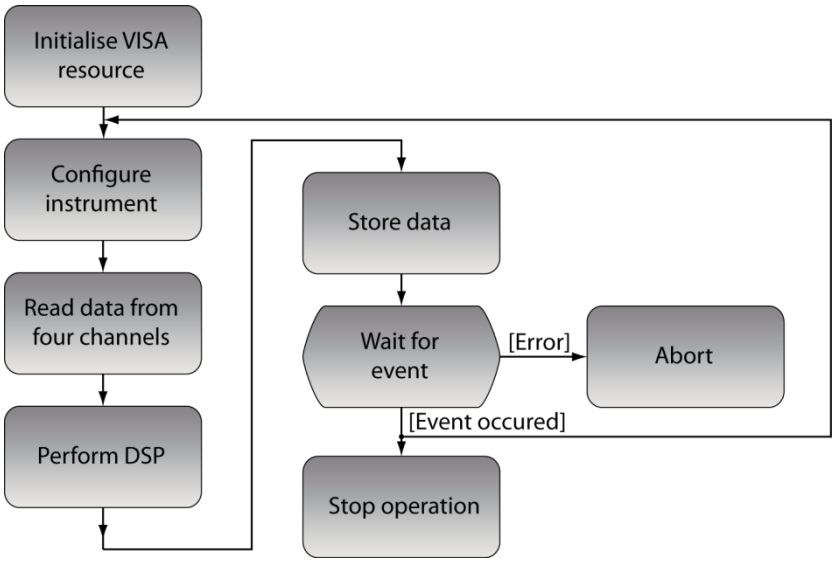

Figure 7.12: Diagram of the execution sequence of the oscilloscope control software.

7.3.5 DAQ software system

Analogue signals recorded by the oscilloscope operating in a real-time mode are digitised and transferred to the PC via USB communication protocol for a further processing. Digital signal processing is performed on-the-fly as the data acquisition and instrument control is made. However, the signal processing does not operate in the real-time mode since MS Windows is not a real-time operating system.

The DAQ software system operates in a sequential scheme, executing multiple functions responsible for an instrument control and data capture. The data capture, display and signal processing functions require adjustments performed live via GUI (Figure 7.13 and Figure 7.15) as the system operates. There are two data paths, separate for each of the sensor subsystems. The data set captured form the Coulter counter sensor subsystem is on-the-fly processed, displayed and written to a database file (Figure 7.14). While the data set recorded from the ISFET subsystem does not require further processing. Hence, the data are displayed and stored in a database file (Figure 7.16). The data captured from the two sensors is stored in a comma separated values (CSV) formatted file. Off-line postprocessing of the data is required to recover information from the signals. These are; electrochemical response of the sensor, drift, hysteresis, and cell count rate.

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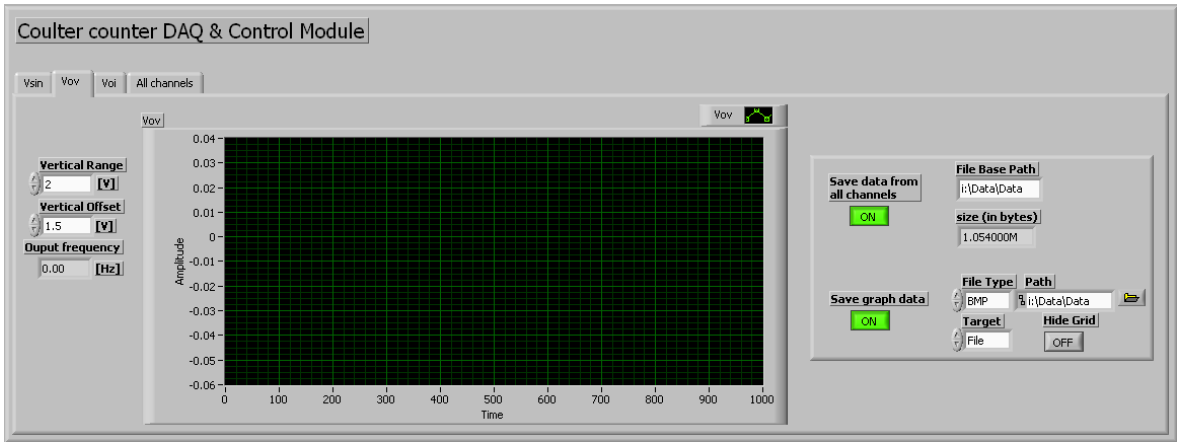

Figure 7.13: GUI of the DAQ module of the Coulter counter subsystem.

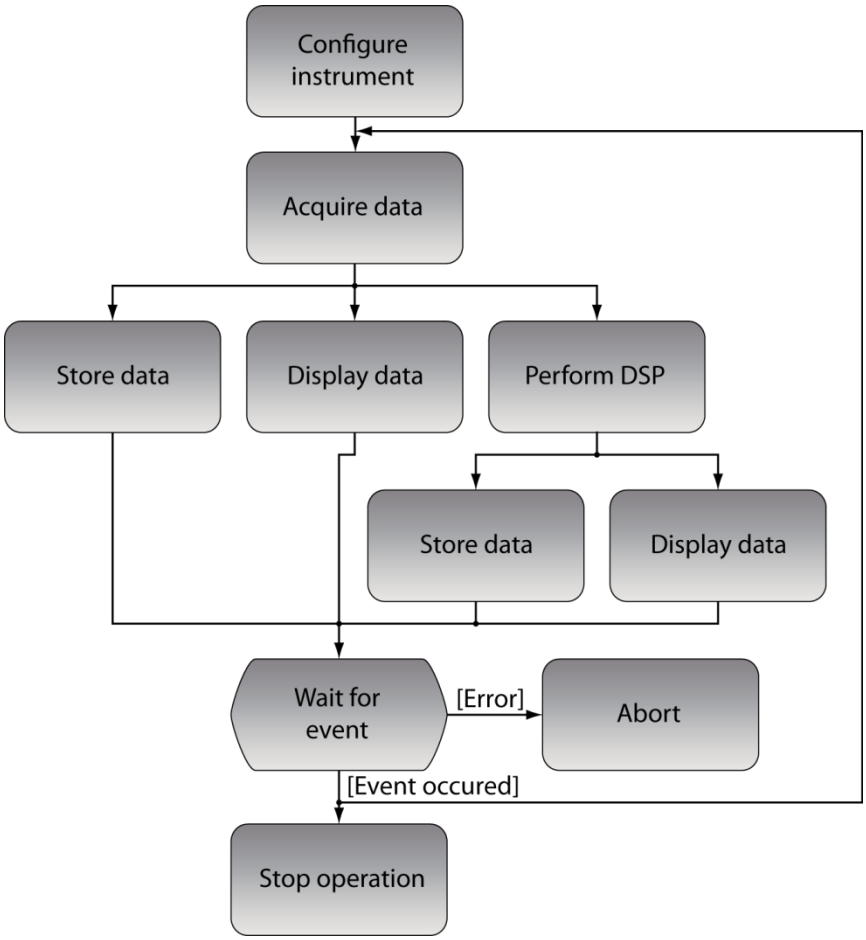

Figure 7.14: Diagram of the execution sequence of the DAQ software recording data from the Coulter counter subsystem.

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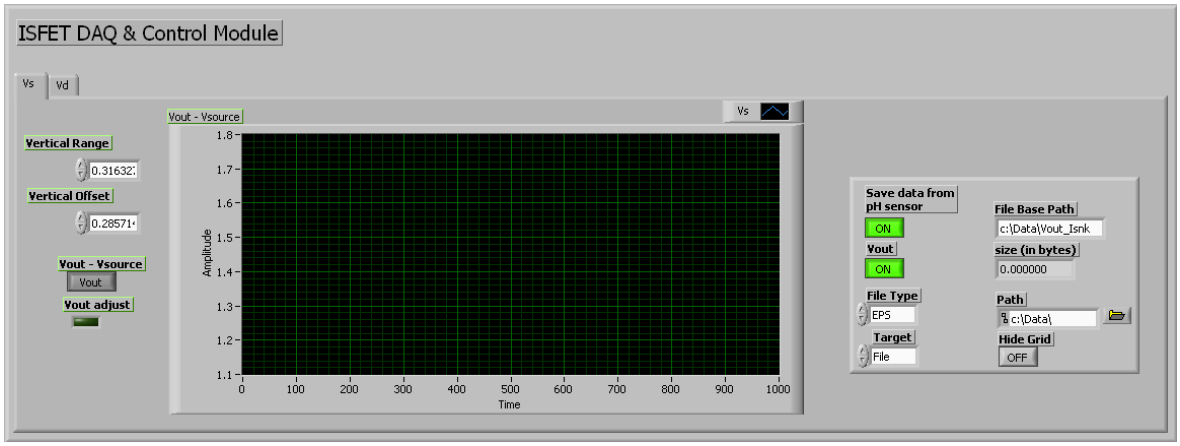

Figure 7.15: GUI of the DAQ module of the ISFET subsystem.

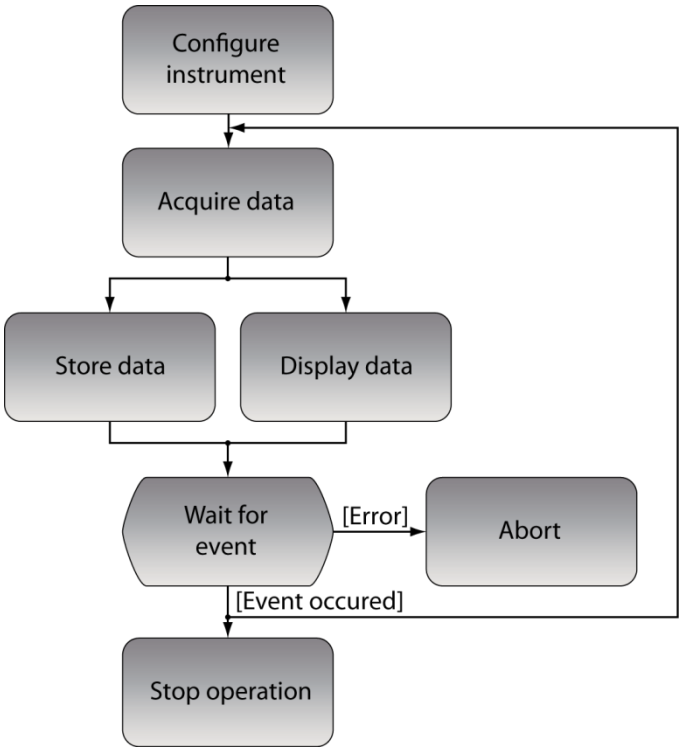

Figure 7.16: Diagram of the execution sequence of the DAQ software recording data from the ISFET subsystem.

7.3.6 DSP module

Analogue signals acquired from the Coulter counter subsystem are digitised by the oscilloscope. Digitised sinusoidal signals carry the information in terms of the amplitude modulation. To recover the information signals are processed in the digital domain. Amplitude demodulation is performed on-the-fly by the DSP module. This module uses GUI (Figure 7.17) to tune the parameters of the amplitude demodulation algorithm (Figure 7.18).

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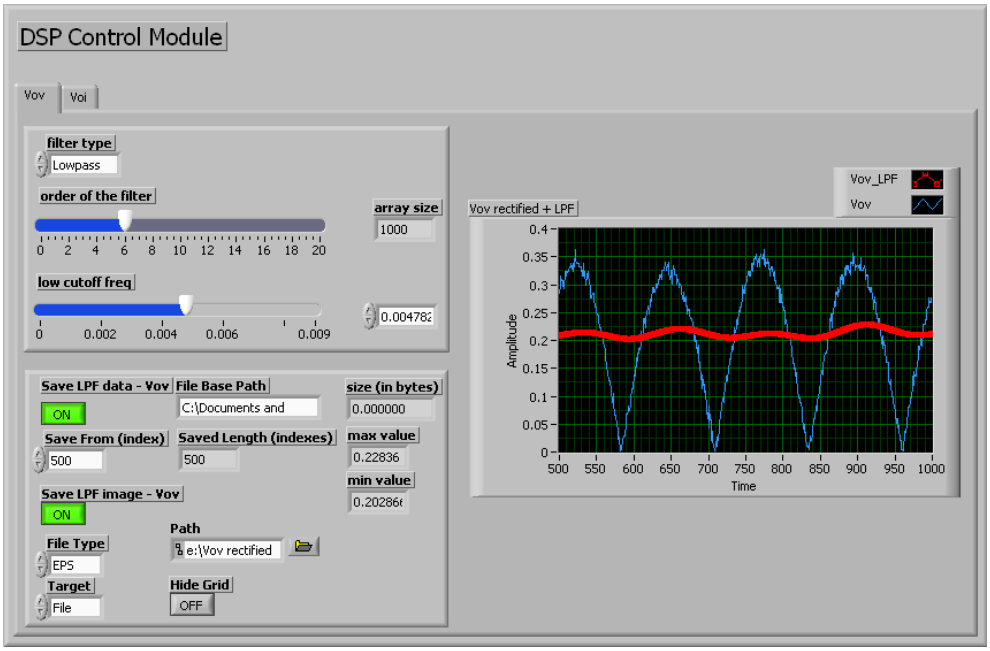

Figure 7.17: GUI of the DSP module.

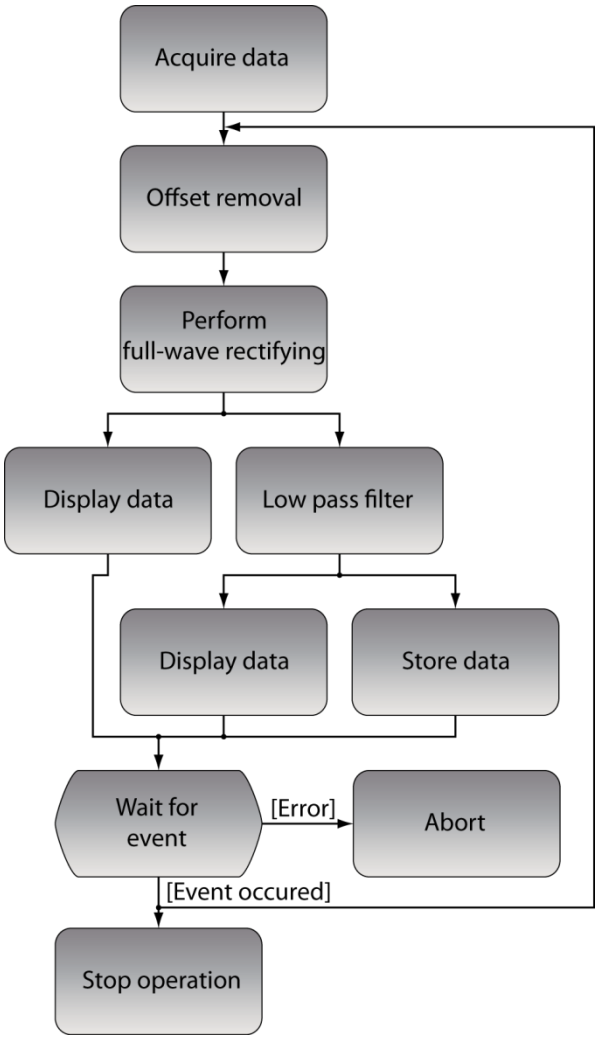

Figure 7.18: DSP algorithm.

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The signal processing requires several steps to recover the information related to the variation of the pore's impedance. The process is initiated by removing the DC offset from the signals. In the next step the sinusoidal signals are full-wave rectified by taking the absolute value. To retrieve the amplitude of the rectified 400 kHz signal, the data is passed through a 6^{th} order Butterworth low pass filter with a cut-off frequency of 400 kHz. Consequently the variation in pore's impedance can be recorded in terms the DC component value change. After processing the digital data are displayed and stored in a database file.

7.4 Experimental procedure

With successful completion of the preliminary set up and calibration procedures (see Section 6) of the apparatus, a wet chemistry experiment is carried out. The developed cytometry system including hardware and software cooperation is applied to the demonstration of the living cell detection. Two integrated sensor arrays (see Section 4) are used to detect cells in terms of their physical size and surface charge agglomerated onto a plasma membrane. Each sensor subsystem is used separately since simultaneous operation of the two is not possible with the current design. For both flow-through sensors the same aperture size of 10 μm x 10 μm is utilised since it gives highest probability of detection (see Section 6.4 and 6.5) of the RBCs which are 6 – 8 μm in diameter and 2 μm thick. The sensors embedded into this particular aperture are enabled by issuing of the logical combination (0000) on the digital addressing lines *A1*. . . *A4* or *D1*. . . *D4* (see Section 4.3.6) for the two sensors respectively. Furthermore the ion sensor uses SiO_2 charge sensitive membrane due to its greater electrochemical response towards alkali solutions, as it was measured during sensor characterisation (see Section 6.5). This should produce a larger response of the ISFET when used to detect RBCs with negative charges carried on their plasma membrane [171]. Bias condition and stimulus parameters remain as for the device calibration. Once the electronic configuration including stimulus and bias conditions is completed a flow cytometry experiment is initiated. As a prerequisite to the experiment, the CIP is performed with DI water to remove any impurities and air bubbles from the microfluidic system. Thereafter the analyte sample is supplied from the 20 ml syringe (Becton, Dickinson and Company) controlled by a syringe pump. Fluid flow rate is set to 3 μL/min and is maintained constant throughout the entire experiment.

7.4.1 Analyte sample

The analyte sample contains ovine RBCs (Figure 7.20) suspended in the 0.1 molar NaCl that was buffered with RPMI 1640 culture medium. An initial cell concentration of 1,000,000 cells/μL was diluted to 100,000 cells/μL. The RBC is a primary carrier of oxy-

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gen (O_2) (> 98 %) and one of the three carriers of carbon dioxide (75 %) within the organism [172]. The carbon dioxide (CO_2) which is a resultant of a metabolism in the tissue diffuses into RBC (Figure 7.19 (a)). It binds with haemoglobin (*Hb*) proteins (Figure 7.21) but the majority of the CO_2 combines with water to form a carbonic acid (H_2CO_3) (Equation 7.1). The reaction is accelerated by an enzyme, carbonic anhydrase. In the next step the carbonic acid dissociates into hydrogen (H^+) and bicarbonate (HCO_3^-) ions (Equation 7.2) [172].

$$CO_2 + H_2O \leftrightharpoons H_2CO_3 \tag{7.1}$$

$$H_2CO_3 \leftrightharpoons H^+ + HCO_3^- \tag{7.2}$$

Hydrogen ions bind to reduced haemoglobin once the oxygen is released. Hence removing the free hydrogen ions from the solution may raise the osmotis pressure within the cell, causing the rupture of the membrane. The Bicarbonate ions diffuse out to the plasma and are exchanged for chloride ions (Cl^-) to maintain the electrical neutrality. Hydrogen ions are unable to diffuse out and are contained inside the cell. Intercellular pressure increases by a small amount and water (H_2O) enters through the plasma membrane causing the cell to swell. A reverse process takes place (Figure 7.19 (b)) once the red blood cell circulates through the lung tissue (alveoli). Haemoglobin molecule reversibly binds to an oxygen gas diffusing into the cell, this allows it to pick it up in the lungs and release it in the tissues [173, Chapter 3]. The association of the oxygen with the haemoglobin is facilitated by the histidine group (HbH).

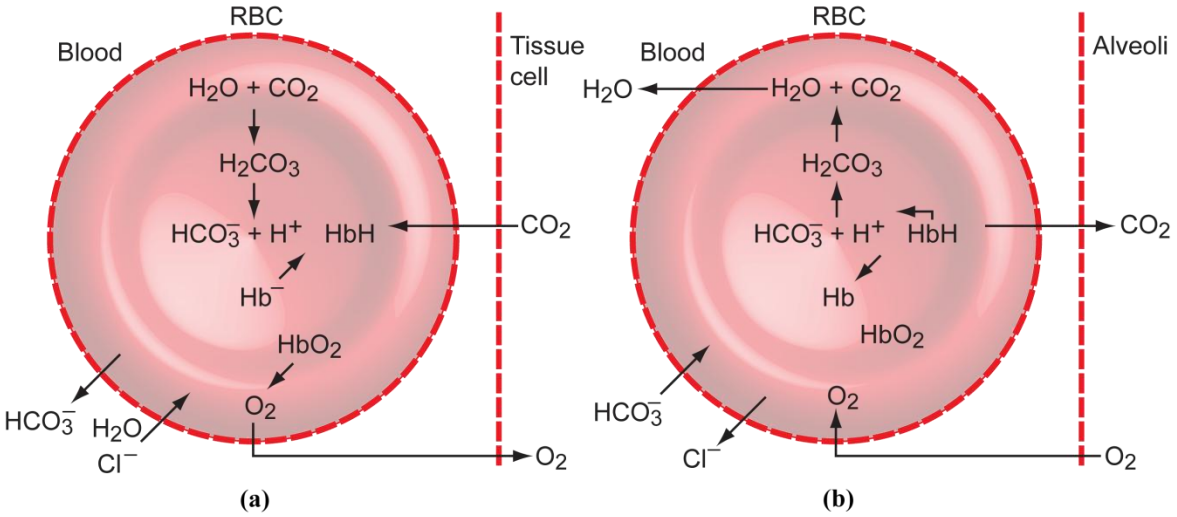

Figure 7.19: Movement of gases at (a) tissue and (b) alveolar level [172].

Decrease in the CO_2 content within the RBC increases its pH index and in reverse, increase in the CO_2 content decreases the pH index of a cell. Furthermore, the transfer of the

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charged species through the cell's membrane modulates the ionic composition stored on the plasma membrane. Hence recording the plasma membrane charge allows to measure respiratory mechanism within the living body [174].

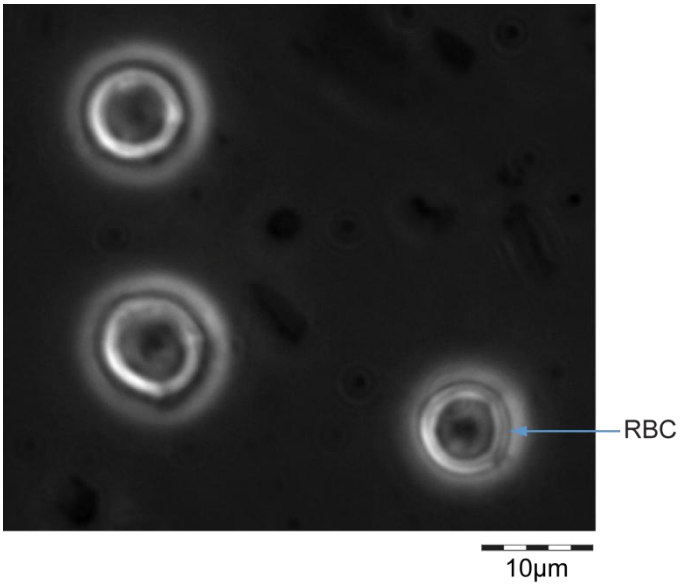

Figure 7.20: Microphotograph of the ovine RBCs in suspension.

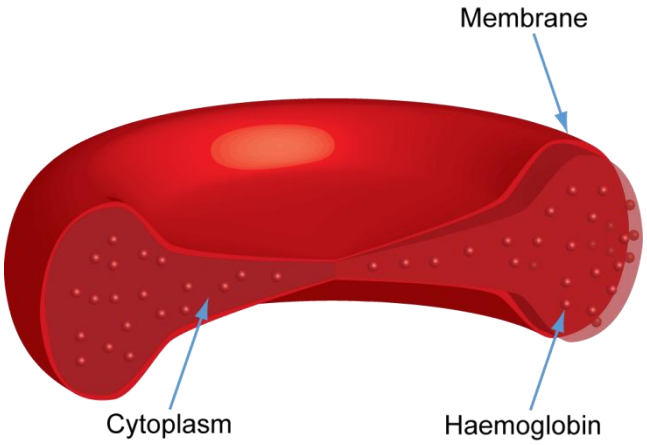

Figure 7.21: RBC cross-section.

7.4.2 Results and discussion

The introduction of the ovine red blood cells causes two phenomena to occur in the flow-through sensor arrays. Consider the AC Coulter counter. Impedance measurement of a healthy cell at a frequency of 400 kHz is dominated by the cell membrane (Figure 7.21) capacitance (see Section 2.3). By measuring the micro-pore's impedance, capacitance modulation was recorded due to the cell's presence in the sense micro-aperture (Figure

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7.22). The ionic composition in the micro-pore is measured by a flow-through ISFET, therefore the modulation in the ionic species due to the presence of the cell in the sense aperture (Figure 7.22) was recorded in the real-time. Thereafter, the recorded signals are displayed and stored on-the-fly by the DAQ and control system.

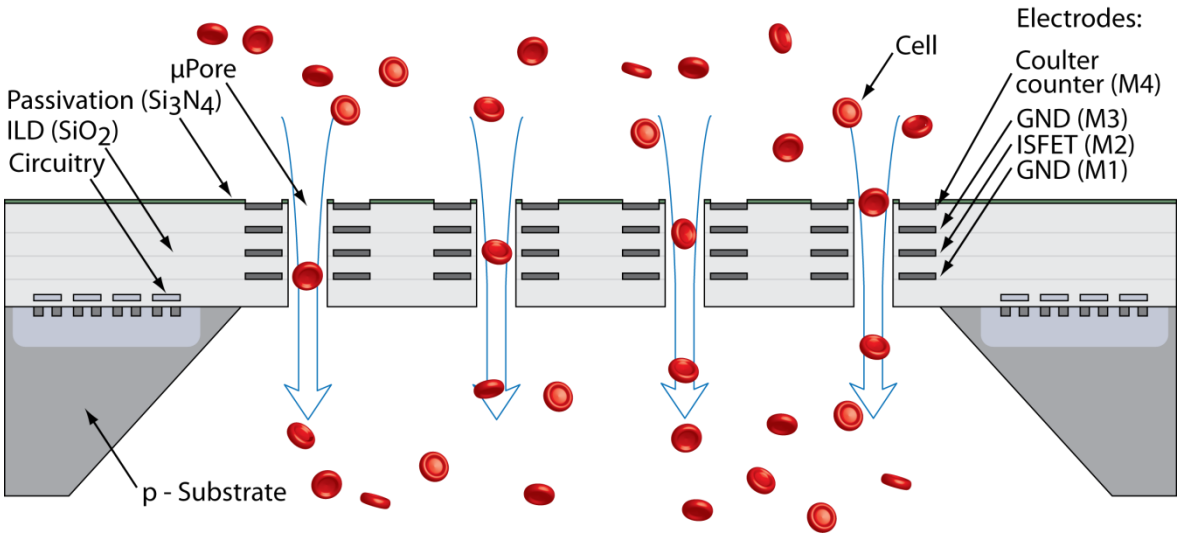

Figure 7.22: Cross-section through the on-chip membrane, showing RBCs flowing through the sense micro-apertures.

For the Coulter counter subsystem operation, only the output voltage, V_{OV}, from the op-amp, A_1 (Figure 6.10) was recorded while the experiment ran. The instrumentation amplifier, A_2 (Figure 6.10) did not produce a desired response significantly above the noise level that could be linked to the detected cell. Hence its output voltage was not considered during the flow cytometry experiments. Data extracted from the impedance sensor subsystem shows a succession of short pulses (Figure 7.23 (a)). The data recorded by the ISFET sensor subsystem also shows the number of pulses (Figure 7.23 (b)). However these pulses are of various widths which may be accounted for by the cells adhering to the dielectric membrane. Note that because the two sensor arrays require different bias conditions the measured data was not acquired simultaneously. From the experiment, it is observed that for each sensor type the data clearly shows a pulsatile waveform, where each pulse corresponds to the presence of a red blood cell in the micro-pore. For the Coulter counter the pulse width is very similar for each event and is on the order of 1 ms. The pulses have a height of approximately 26 mV after DSP processing (see Section 7.3.6). Such amplitude of pulses produced by the sensor readout electronics is sufficiently above the noise floor of the system to be detectable. For the pH sensor subsystem the recorded signal is considerably more clear with the pulses have a height of 435 mV. The Coulter counter operates at a modulation frequency above the 1/f noise corner for the MOSFETs deployed, whereas the

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ISFET based ion sensor would expect to be vulnerable [144, 175]. However this does not appear to be a threat, as indicated experimentally. For the ion sensor however, there is a considerable variation in the pulse width. This could be an indication of the amount of time each red blood cell spends inside the micro-pore, but if that were the case then similar results would be expected for the Coulter counter. Therefore, it can be hypothesised that the variation in pulse width arises from factors owing to the charge sensitive nature of the device, as well as the ionic species dissociation from the charge sensitive interior of the micro-pore. When a red blood cell enters a micro-pore it transfers charge to the pore sidewall, hence modifies the surface charge stored on the floating gate of the ISFET electrode. In the absence of any further perturbation the measured signal will not change until another cell arrives.

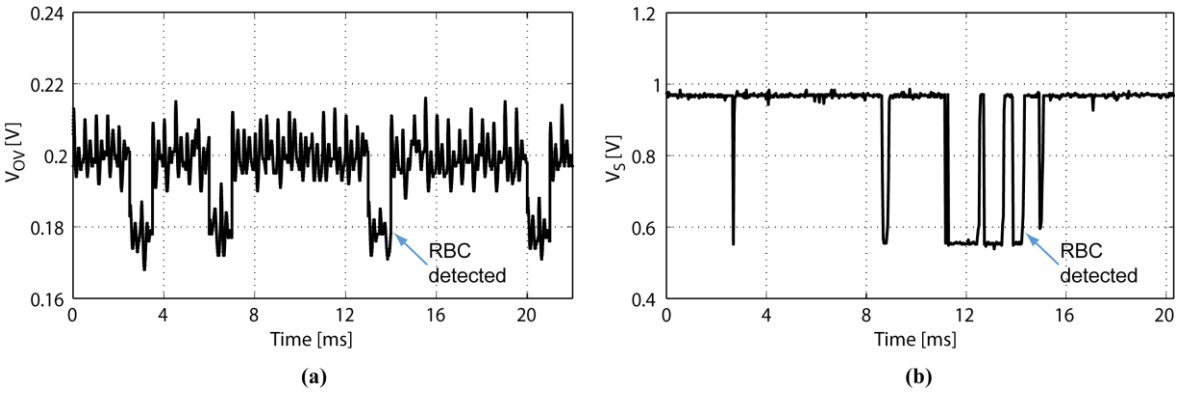

Figure 7.23: Output voltages from the (a) Coulter counter and (b) ISFET subsystems, showing the amplitude change due to the detected RBCs.

7.4.3 Performance of the SSoC

The performance of the presented device can be compared with that of others [7]. A single micro-channel (20 x 20 μm^2) lateral coulter counter with a sample flow rate ranging from 0.2 µL/min to 2 µL/min and a cell detection rate on the order of 100 cells/s has been presented [176]. A high-speed device has been reported [177] where the polystyrene beads (15 µm) flowed through a 40 µm deep and 200 µm wide micro-channel equating to a total of 30,000 beads/s for the whole device. The CMOS-MEMS device presented in this work has a 4 x 4 flow-through array of micro-pores. All apertures have a Coulter counting flow rate of 3 µL/min, achieving 190 cells/s for one micro-channel (data extracted from Figure 7.23 (a)), therefore the estimated cell count rate for all the apertures is 3040 cells/s. The data illustrated in Figure 7.23 (b) show that the flow-through ISFET sensor can achieve 300 cells/s for one micro-channel, hence, assuming that this approximates to the maximum rate achievable, the estimated cell count rate for all the apertures is 4800 cells/s. In contrast to

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the reported sensors to date, the presented device is integrated together with readout electronics and developed using a commercial CMOS platform. This is one of the factors enabling high scalability, as an example the expected Coulter counting rates of 38,000 cells/s would be possible for the device with 200 sense apertures. The fastest commercially available system achieves 500,000 cells/s, [178] which equates to 2,632 apertures for the device developed in this work. Furthermore scaling on a single chip, and using several chips in one machine, there is potential to exceed the performance of the current state-of-the-art methods using low-cost CMOS-MEMS technology, with the potential for miniaturisation into a handheld format. Besides that the developed device allows the recording of a number of parameters of the living cells. This enables a multi-parametric *in vitro* analysis of a cell population which gives a possibility for a greater insight into cell metabolism and health state [3] in a device of a small form factor.

7.5 Summary

In this chapter, a complete cytometry system was realised by simultaneous co-design of the software and hardware systems. Hardware system encompasses the sensor-system-on-chip, test & measurement instrumentation, PC, and the microfluidic subsystem. Modular design enabled quick replaceability of the package CMOS-MEMS module. The measurement system was automated by a DAQ and control software system running on the PC. Data was captured separately for each of the sensor subsystems. A cell detection experiments were then carried out with the developed cytometry system. Finally the developed system was compared with the current technology. The next chapter summarises the presented work and draws the conclusions from the research together with ideas for further improvement to the system and hints for future work.

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8 Conclusion and Future Work

8.1 Introduction

In this thesis, the design, implementation and use of a novel CMOS-MEMS cytometry system incorporating a Coulter counter and ISFET-based sensor was described. Detection of single living cells was demonstrated using the prototype of the measurement system. This section concludes presentation of the research work and provides suggestions for the next generation flow-through CMOS-MEMS device for biological cells and micro-particle sensing.

8.2 Research Work Final Remarks

The presented work has focussed on the development of a Sensor System on a Chip utilising state-of-the-art microtechnology for single cell detection. The measurement system concerned a CMOS electronics design together with implementation of the sensor system on the same silicon substrate. Furthermore the CMOS compatible post-processing techniques were applied to enable a flow-through device operation, so that the developed MEMS could perform multi-parametric cytometric measurements. The working prototype of the system has been created, although due to its complex operation a number of obstacles were encountered and overcome during development.

8.2.1 CMOS integrated electronics and sensor system

The CMOS-MEMS device was designed using the Cadence tool chain. Utilising EDA software the schematic capture thereafter schematic-driven-layout was performed at both transistor and standard library cell level. In order to verify and tune the circuit behaviour computer simulations were used. This was enabled by using the Spectre circuit simulation tool in the design process. The IC design was carried out using a commercial 0.35 µm 4-Metal, 2-Poly CMOS process technology. The process design kit and foundry service were supplied by *austriamicrosystems* AG. The technology kit allowed custom design to be implemented together with standard analogue and digital cells. Incorporation of both led to an ASIC integration with the two flow-through sensor arrays. For initial prototyping the 0.35 µm technology node was well suited and allowed an efficient in-house post-processing, however the device has the potential to be scaled in multiple directions. Using latest technologies, with their nodes in the sub-nanometre range, the electronic circuitry can be scaled down, so that less of the chip area is consumed. On the contrary, the flow-through sensor arrays are not easily scalable down in size (micro-channel diameter depends on the

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analyte physical dimensions); however the number of micro-channels can be multiplied extensively enabling higher throughput.

The flow-through sensor system consisted of a two stacked 4 x 4 micro-channel arrays embedded into an on-chip membrane. The Coulter counter's microelectrode array implemented on Metal 4 was exposed directly to an analyte solution by opening the passivation over the Metal 4 layer. On the other hand the ISFET's floating-gate microelectrode array was insulated by an intra-layer-dielectric (SiO_2) lining the inside of the micro-pore. The Coulter counter (impedance sensor) readout circuitry was based on a bridge topology and the ISFET based ion sensor readout electronics was based on a source-and-drain follower. Each of the ISFETs was designed as a floating gate p-MOSFET. This added additional noise immunity, since the p-type transistor was embedded into an n-well which developed a reverse biased diode (around the ISFET) with a main p-type substrate. Furthermore, the source and bulk terminals of each ISFET were connected together to remove the body effect which causes the threshold voltage to rise. Both arrays were addressed electronically using analogue multiplexers so that a single set of a readout circuitry could be used for each of the sensor sets. Furthermore this enables arrangement a single analogue output for each of the two arrays. In addition this minimises the physical layout area of the circuitry.

The in-house post-processing was carried out at a chip level to create an on-chip membrane and open the micro-pores. The silicon die size (5 mm x 5 mm) was dependent not only on its electronic circuitry features, but it had to be suitable for further post-processing. This was related to the fact that the physical size and shape of a chip highly influences the in-house post-fabrication. The smaller the chip area the more difficult it is to perform DRIE due to the difficulties connected with the resist mask deposition process. Hence it is envisioned that for a next generation of the device the physical size of the chip can be decreased to 4 mm x 4 mm without affecting the capabilities of the sensor system or degradation in the post-processing methods.

The principle of operation of the AC Coulter counter relies on modulating impedance of the micro-pore due to the analyte sample (microparticle or cell) flowing through it. Stimulus frequency has a significant influence on measured properties of the analyte (see Section 2.3.1). In the current design the stimulus frequency was below 1 MHz due to an operational amplifier (OP_LN [141]) used in a readout circuitry. However to overcome this limitation another op-amp able to operate at higher frequencies (i.e. OP_WB [179]) can be used instead. Which as a result can output more information about the cell's electrical properties. A flow-through ISFET is capable of measuring of the ionic concentration within the sense aperture. Hence if a cell with a significant surface charge (agglomerated

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on a plasma membrane) enters the sense micro-pore, the concentration of the ionic species adsorbed onto the pore's sidewalls is altered which causes the modulation of the threshold voltage of the ISFET. The ISFET array was connected to the source-and-drain follower to maintain constant source-drain voltage, while the drain current of the ISFET was held constant by a current mirror. This solution works well with the 4 x 4 array. However increasing the number of the flow-through micro-channels (pixels) thus ISFETs would require to use an additional set of the readout circuitry. Therefore, the silicon chip area consumption will increase. Instead of using a source-and-drain follower configuration the simpler source-follower circuit topology can be implemented. This will reduce the number of parasitic components contributing from metal interconnects and simplify the routing of an array consisting of a large number of flow-through apertures.

The physical layout of the circuitry and sensor system was designed by applying device matching principles (et al. symmetry and orientation rules) reducing the influence of the manufacturing process variation on the device properties. Further improvement can be introduced by rearranging the on-chip physical circuitry closer to the two sensor arrays (more compact design), hence reducing the wire length between the sensor and readout electronics and thus minimising the interface (sensor-readout electronics) wire parasitics. This would be closely related to the post-processing method modification which is discussed in Section 8.2.2. Each electronic subsystem layed out around the sensor arrays was screened by a guard ring. This provided protection to the analogue circuitry against noise coupled through the bulk silicon as well as isolated the digital part of the circuit from introducing the noise into the substrate. This protection can be further enhanced by using multiple guard rings especially around the ion sensor subsystem, it can also improve ISFET drift immunity.

The four flow-through electrode stack (two sensing and two screening electrodes) in each of the sense micro-pore designs have outside dimensions on the order of 100 μm x 100 μm with a variable size of the inside (of the electrode) opening (see Section 4.3.7). The distance between adjacent electrodes was constant and set to 33.3 μm. This distance can be further decreased enabling a higher micro-pore density in larger arrays. It will also require using of a more efficient routing method of the interface wires. The electrode stack design (inside opening in a metal plate) was closely related to the micro-pore (located in the centre of the electrode stack) size which in the present work was in the range from 10 μm x 10 μm to 16 μm x 16 μm.

Design for test (DFT) methodology was applied during the IC design phase. This relates to the number of test points introduced in the physical layout of the device enabling easy debugging during device characterisation. Critical components of two subsystems

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were also layed out separately for further debugging in case of invalid operation of the system. These features consumed silicon area and increased the complexity of the device packaging. Since all of the subsystems operated and were able to perform the analyte measurement the DFT methods can be abandoned for further designs decreasing the chip area and improving the microfluidic packaging ability.

8.2.2 Chip level post-processing and packaging

Post-processing was one of the key counterparts of the sensor system development. Flow-through sensor operation (micro-pore opening) was enabled in a two stage process. First, the front-side of the chip was etched creating the micro-pores in the passivation (Si_3N_4 and SiO_2), inter-layer-dielectrics (SiO_2) and pre-metal-dielectric (BPSG) layers which were 8 μm in depth. Micro-pores are located in the centre of each of the micro-electrode stacks. Secondly the back-side substrate (silicon) was etched creating the on-chip membrane as well as opening the micro-pores.

For the front-side processing two different methods were tested (one at a time); reactive ion etch and focussed ion beam. Each of the two methods has pros and cons (see Section 5.2.1). The RIE requires a multilayer resist mask to enable deep oxide etch while the FIB does not require any mask. However the RIE is a parallel process (all pores being etched simultaneously) where the FIB is serial (one pore being milled at a time). In the RIE process bigger openings are etched faster because more reactive plasma can get into the wider etch window rather than into the narrow one. On the other hand the FIB uses a narrow beam of highly accelerated ions (gallium) to remove a material from a sample surface. With the ion beam spot size in the sub-micrometre range (~ 0.3 μm) it was observed that the process is efficient with milling the micro-pores of a diameter less than 20 μm. In comparison to the RIE the FIB milling of sixteen pores (ranging from 10 μm x 10 μm to 16 μm x 16 μm in size) took 139.2 min. Etching in a reactive plasma of a sample with the similar mask openings and the desired etch depth of 8 μm took 3 h, however process had to be split into six runs due to machine properties. This resulted in a much longer processing duration using RIE to etch one sample at a time. A large number of samples etched at the same time in the reactive plasma would be the desired solution however this is not the case in the presented work. The FIB milling time can be further decreased by sputtering the sample material only around the perimeter of the desired opening shape (Figure 8.1(c) and (d)). For instance in comparison to the current method (Figure 8.1(a) and (b)) the time required to etch a micro-pore larger than 15 μm in diameter will be significantly reduced by using proposed solution. Milling time for the two methods (“current” and “proposed”) is provided automatically (once the desired etch pattern is given) by the machine control

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software. Therefore the processing time can be verified prior to the etch process, thus a more time efficient method can be applied. Hence the use of the proposed method will be more time efficient if:

$$A_C > A_P \tag{8.1}$$

where A_C is the size of the surface area etched by current approach and A_P is the size of the surface area etched by proposed approach.

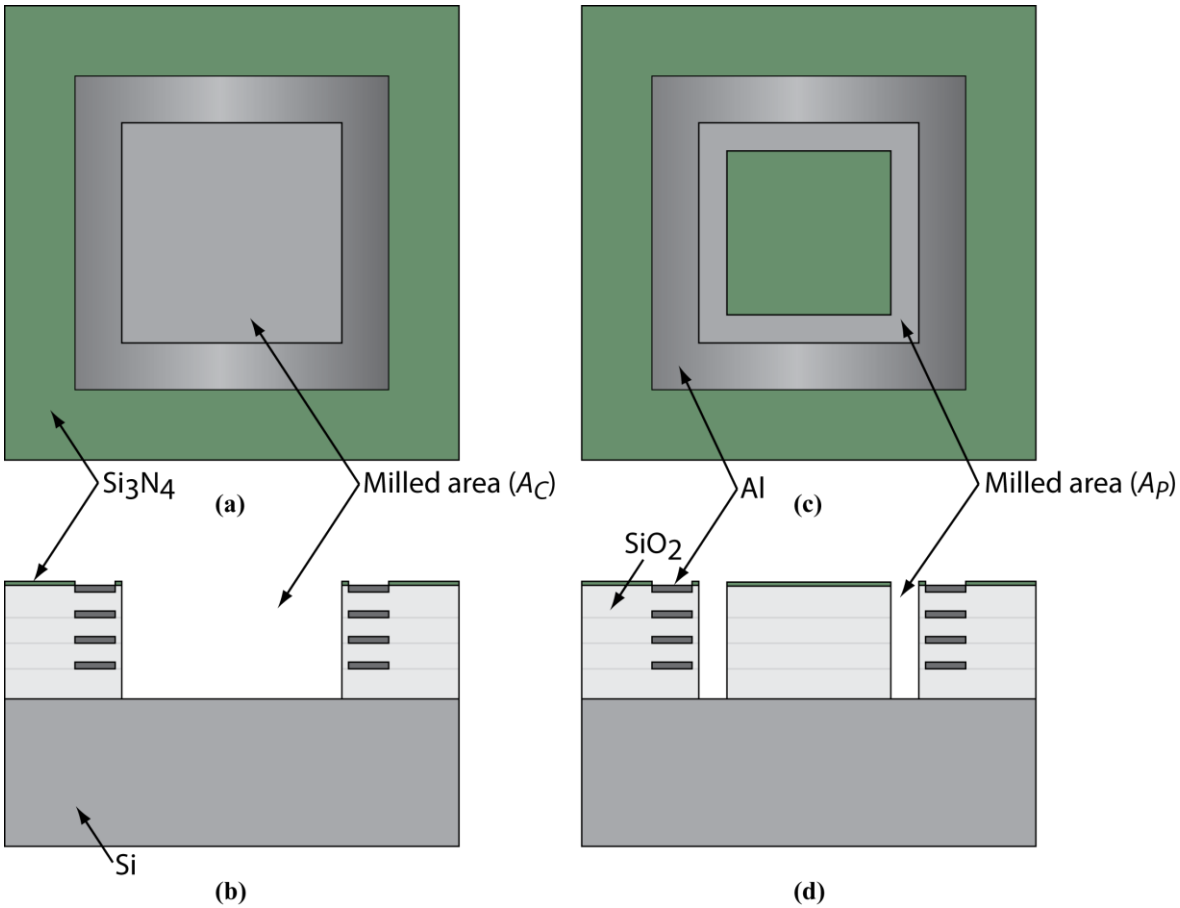

Figure 8.1: Front-side FIB milled micro-pore using the two methods. (a) Current method – top view, (b) Current method – cross-section, (c) Proposed method – top view, (d) Proposed method – cross-section.

Since the back-side silicon etching using the DRIE-ICP process will be carried out after front-side FIB milling, the material (Si_3N_4 and SiO_2) remaining in the pore will be removed together with the underlying substrate, hence fully opening the micro-pore.

During the thick film multi-layer mask development for the RIE processing the square mask windows (for the micro-pore openings in the Si_3N_4 and SiO_2) tended to round (at the edges and corners) due to thermal processing (multiple baking) of the resist. Therefore it is reasonable to design the openings in the photolithography mask as circular windows if RIE has to be utilised. A rounded aperture will be etched (by RIE) more uniformly

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producing smooth sidewalls with the desired opening shape. On the other hand the FIB processing can produce openings with various patterns without degrading the micro-pore profile. Precision gained with the FIB milling, rapid processing (no requirement for prior preparation of the device) and a user control (in real-time) over the etch process makes it more suitable for the current research work. Hence it is suggested for future prototyping to use FIB for the deep oxide etch.

Back-side etch was performed using DRIE-ICP to remove the silicon substrate underneath the entire on-chip membrane which in consequence led to the opening (in the bottom) of the micro-pores. The required substrate area to be removed had dimensions of 800 µm x 800 µm, the etch depth was defined by the wafer thickness (on which the device was fabricated) which was on the order of 525 µm (see Section 5.2.2). A photolithographically developed multilayer resist mask was required to define the etch window. For an UV exposure of the resist mask a back-side alignment (BSA) mode was used. To enable precise BSA a set of markers was utilised (Figure 5.2 and Figure 5.5). The set of markers in the form of crosses was developed on the substrate while a front-side processing. These were aligned (while BSA) with the set of complementary markers on the back-side photolithography mask (Figure 5.5). This process can be significantly improved by embedding the top-side alignment markers on one of the metal layers during the IC physical layout design phase. The set of markers should be symmetrical as well which would make the alignment process easier. This can be done by placing one marker in each corner of the chip layout. Specific bond-pad-ring (also referred to as power-ring) design makes this area unused as is shown in Figure 8.2.

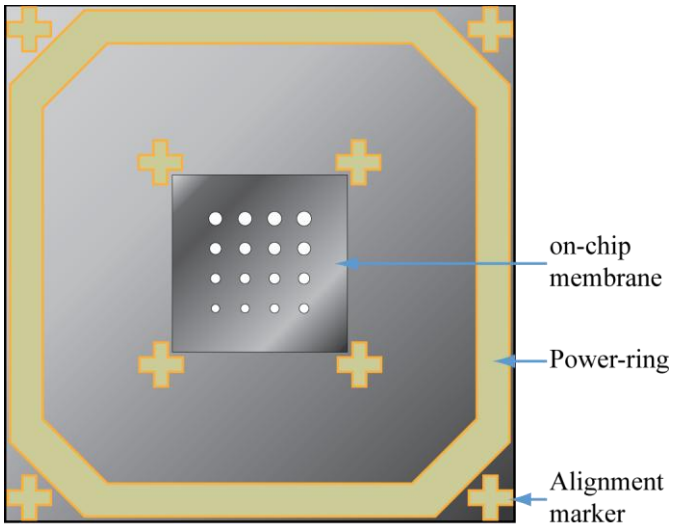

Figure 8.2: Layout of the markers for the back-side alignment.

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The another set of alignment markers can be layed out in a close proximity to the on-chip membrane (in the space unused by the circuitry to avoid interference) to further increase the back-side alignment precision as well as highlight the perimeter of the bottom side etch window.

Once the DRIE-ICP process was finished the on-chip membrane with embedded micro-pores was released, the thickness of which was 8 µm. This thickness, in conjunction with a relatively large area (800 µm x 800 µm), made it fragile and vulnerable to excessive pressure especially during flow-through test and measurement experiments and as a consequence limiting the lifetime of each of the CMOS-MEMS devices. To overcome this limitation the on-chip membrane design can be improved by developing an appropriate back-side etch pattern. The proposed mask window area for each of the back-side openings (underneath each of the micro-pores separately) would be 100 µm x 100 µm. This is in an achievable range of a high aspect ratio DRIE-ICP in conjunction with a custom developed thick film resist mask (see Section 5.2.2). However instead of using 525 µm thick wafer as for the current device, thinner silicon wafers (375 µm) can be used by requesting at the design tapeout phase (feature supported by *austriamicrosystems* AG). Reduction in substrate thickness by 28.6 % (Figure 8.3) will enable faster back-side processing by decreasing the number of thick film resist layers needed (two instead of four) for the mask as well as significantly reducing the ICP etch time. Removing the silicon only underneath each of the micro-pores will leave enough substrate material between the openings to create a support structure for the entire on-chip membrane (Figure 8.3). This silicon structure will keep the membrane rigid and able to withstand higher pressure, therefore enabling higher flow rates of the analyte solution thus higher throughput of the entire system. Furthermore the proposed membrane design will allow the readout electronics to be layed out closer to the sense micro-pore reducing length of the interface wires thus their parasitic components (reducing silicon die size as well).

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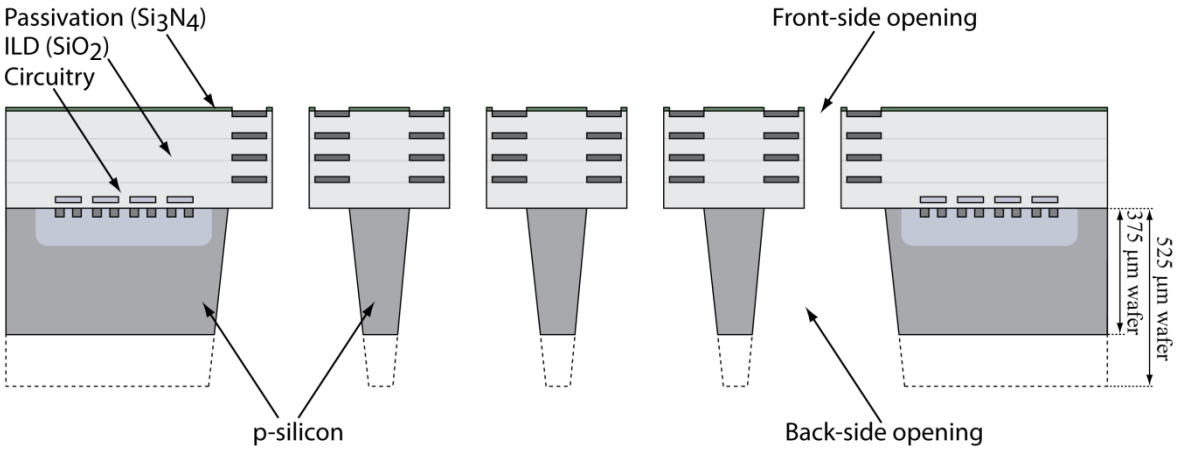

Figure 8.3: Improved on-chip membrane design.

In the next post-processing step the interior of the sense micro-pores was coated with silicon nitride (Si_3N_4) to improve the ISFET electrochemical response. Even better results can be gained coating the charge sensitive membrane (interior of the pore) with tantalum pentoxide (Ta_2O_5) [80]. Thus this material is suggested for a future use.

Custom microfluidic encapsulation and packaging was a key aspect of this research work. The flow-through operation of the measurement system was enabled by a CMOS-MEMS device encapsulation onto the custom PCB chip carrier followed by a top and bottom-side packaging of the module. In the current system design this approach was preferred over the standard ceramic IC package because the custom PCB design gave more flexibility with a microfluidic encapsulation for the flow-through mode of the sensor system operation. A double sided PCB chip carrier was supplied with a custom made recess and a macro-fluidic channel so that a fluidic system could operate.

However for future designs a standard IC package can be used i.e. ceramic pin grid array (CPGA) together with a complementary PCB mounted socket i.e. zero insertion force (ZIF) PGA socket simplifying the entire packaging process. The ceramic IC package still needs to be post-processed to open the macro-fluidic channel at its bottom to enable flow-through mode of operation in the measurement system.

After applying glue in the milled recess, the CMOS-MEMS device was positioned in its centre and precisely aligned with a macro-fluidic channel. In the next step the on-chip bond pads were connected with tracks on the PCB using aluminium wires with a diameter of 25 µm. Once finished a microfluidic encapsulation was performed followed by a front and bottom-side packaging. An issue arose while encapsulation using epoxy potting compound. Exposed and electrically conducting parts on the chip (except the on-chip membrane) were required to be insulated, since the process was carried out by hand the test points layed out in a close proximity to the on-chip membrane causing difficulties due to

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the danger of damaging it by enclosing the sense apertures with glue or by mechanical fracture. To prevent this, it is proposed for a future device design that any overglass opening, either bond pad or test point should be positioned as far as possible from the sensor array design.

Packaging was done using PEEK NanoPort connector (Upchurch Scientific, Inc.) and cable gland for the front and bottom-side respectively. The bottom-side package was housed in a fixed position along with the Ag/AgCl reference electrode. Aqueous analyte solution supplied from the syringe controlled by a pump was introduced through the front-side NanoPort connector and drained from the bottom-side package to the waste container. During a calibration and experimental work it was observed that the lifetime of the encapsulation as well as the package, exceeded the lifetime of microfluidic operation of the CMOS-MEMS device itself. Therefore it is suggested to focus on the miniaturisation of the entire package so that potentially utilising smaller front and bottom-side containers together with a miniature reference electrode could be used enabling faster analyte flow-through and decreasing the footprint of the measurement system.

8.2.3 Sensor-system-on-chip characterisation

The calibration of the sensor system technology was presented in Section 6. Prior to the calibration, the experimental procedure was investigated to ensure that the device operated in desired working conditions. In the next step a microfluidic system flow-through mode of operation was verified. Thereafter electronic operation of each of the two sensor subsystems was tested and calibrated separately. Calibration started by connecting a test & measurement instrumentation setup applying ground loop prevention methodology. First the Coulter counter subsystem was calibrated. The components of the Coulter counter, an array of the flow-through sense micro-apertures and readout (bridge) circuit were characterised separately. Discrepancy between expected and measured on-impedance of the multiplexers was on the order of 12 % which was linked to the manufacturing process variation. This mismatch between nominally identical components could be reduced by further optimisation of the physical layout of the device. However, it was not crucial that these components were well matched since the key objective was to detect the variation in the sense aperture impedance which was on the order of several MΩ. Once operation of each subsystem was verified, the two counterparts were characterised while working simultaneously. The characterisation was performed for two different aqueous analyte solutions introduced to the microfluidic system. For further analysis, a sense aperture size of 10 μm x 10 μm was selected since it would provide the highest probability of detecting red blood cells which are 6 – 8 μm in diameter. The calibration of the Coulter counter subsystem showed that the on-

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chip readout electronics provided adequate performance for operation in conjunction with the array of the flow-through sense apertures.

A flow-through ISFET based ion sensor array calibration was initiated by assessing a performance of the bias and readout electronics. Bias conditions for the ion sensor array were established to operate the ISFET in the linear region. This enabled a wide operating range for the sensor. Assessment has been performed for four distinct thicknesses of the dielectric membrane. During simultaneous operation of the sensor array and microfluidic system significant noise signal was observed in the output signal. Debugging allowed to resolve the issue by using a high quality DC supply to power the syringe pump. In the next step the electrochemical response of the flow-through ISFET has been measured. The electrochemical response of the sensor was recorded for the two dielectric membrane materials. The default dielectric, SiO_2, lining the inside of the pore produced a sensor response of 13.3 mV/pH for the pH 4 to pH 7 index range and 53.7 mV/pH for the pH 7 to pH 10 index range. Modifying the dielectric membrane material by depositing (~ 100 nm) of the Si_3N_4 produced a more linear response of the sensor. The output signal was on the order of 20.3 mV/pH for the pH 4 to pH 7 index range and 41 mV/pH for the pH 7 to pH 10 index range. The difference in sensor drift and hysteresis were also observed for these two membrane materials. The Si_3N_4 coated membrane showed superiority in both terms.

Since the sensor array was intended to operate as a flow cytometry instrument to detect living cells (6 – 8 μm in diameter) suspended in the aqueous solution, the sense aperture size (10 μm x 10 μm) was selected accordingly to maximise the detection probability. For future designs it is suggested to use a single aperture size (for all pores) closely matched with the analyte dimensions. Positioning metal electrodes closer to the aperture will allow more accurate measurements as well. This implies a thickness reduction of the ISFET's dielectric membrane, hence a pH sensitivity improvement should also be observed.

8.2.4 Flow-through Cytometry System

Sensor-system-on-chip was put into operation with the off-chip instrumentation and a data acquisition system (DAQ). Each of the two sensor subsystems integrated on-chip require specific bias and stimulus condition, hence the ion and impedance sensors were operated separately. The system used instrumentation hardware that included several DC power supplies, arbitrary waveform generator, mixed signal oscilloscope, syringe pump, and PC. The measurement system was automated in both data capture and instrument control. Bidirectional communication between the PC and the instrument hardware system was enabled via three interfaces; USB, USB/GPIB and USB/RS232. A DAQ and control software sys-

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tem running under MS Windows OS use a GUI to adjust and read data from the instruments. The resultant DAQ and control system was able to capture data from the two flow-through sensor arrays with a rate of 10 k samples per second (S/s). Acquired data was processed on-the-fly by the digital signal processing (DSP) module embedded in the software system. For the Coulter counter subsystem further signal processing was required to recover the information. A full wave rectification implemented in the DSP software module enabled amplitude demodulation. This outputs the DC component with an amplitude variation directly proportional to the sense aperture impedance modulation. The ion sensor subsystem did not require further signal processing.

The measurement instrumentation setup was connected utilising coaxial wires, this introduces parasitic capacitance components to the system. In order to reduce the influence of the parasitic components produced by the connector wires the measured analogue signals from the two sensor subsystem can be captured on-chip and converted to a digital domain before being transmitted off-chip.

Integration of both hardware and software allowed development of the flow cytometry system. The system was utilised for living cell detection. The Coulter counter subsystem was used to detect red blood cells suspended in a culture medium. The recorded amplitude modulated signal was on-the-fly post-processed by the DSP module embedded in the DAQ software, to recover the impedance modulation of the sense aperture. The electrical properties of the cell measured with a stimulus frequency of 400 kHz are linked to its physical volume (see Section 2.3.1). Therefore, the recorded events carry the information about the size/volume of the cell.

The flow-through ISFET subsystem used the same DAQ software, however several specific parameters had to be adjusted through a GUI. Moreover, the captured signals did not require further post-processing. Hence the acquired data was directly written to a storage file. The ion sensor subsystem measured the variation in pH index of the sense aperture. This mechanism was utilised for detection of the negatively charged biological cells suspended in an aqueous solution. The recorded signal showed a modulation in the ionic concentration within the sense aperture due to the cell presence. Hence cell detection was enabled according to the charge stored on the plasma membrane.

The readout circuitry of the ion sensor showed good enough performance to be able to detect the charged cells which are relatively large in size. However, to be able to detect small molecules a greater resolution is required. This can be enabled by reducing the noise coupled to the ion sensor. To achieve that, the source voltage should be buffered so that it is de-coupled from the sensor readout electronics.

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Captured data from the two sensors subsystems was stored in two separate database files. For long term measurements the acquired data can produce a very large file size. More efficient data storage can be achieved by implementing MySQL database management methodology.

8.3 Future Work

The emphasis in this work was placed on demonstrating a complete measurement system containing two major subsystems rather than on characterisation of the individual counterparts. Since the work was carried out through several phases; design, post-processing and test bench assessment, this resulted in a number of conclusions that can be implemented in future research to improve the performance of the system.

8.3.1 Electrode layout optimisation

For the current design a square shaped electrode layout was used for both sensors. A square shape sense aperture can be replaced with a circular geometry relatively easily by redesigning the photolithography mask used in front side (RIE) post-processing, while an FIB is even easier due to the software controlled milling process. The on-chip electrode layout can only be changed by redesigning the CMOS chip. Circular shape electrodes (Figure 8.4) implemented for both the Coulter counter and ion sensor will improve the electric field line arrangement across the sensing surface of the corresponding electrode area.

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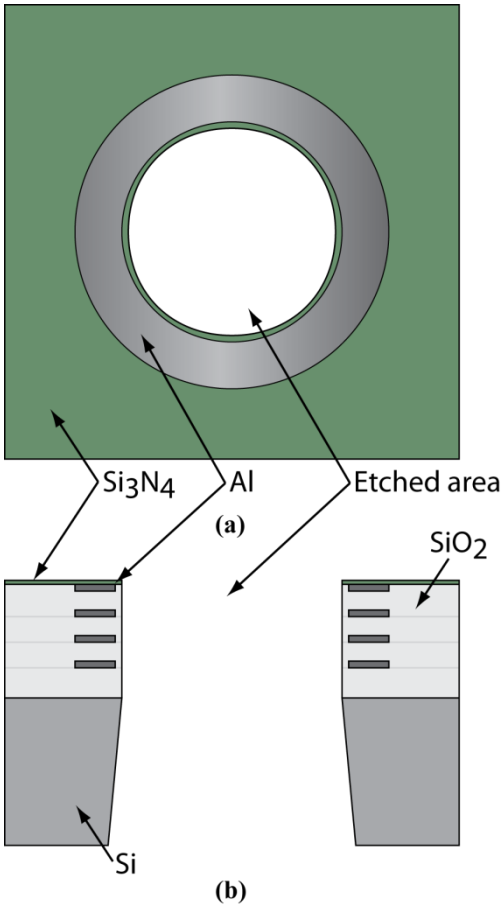

Figure 8.4: Circular electrode stack. (a) Top view, (b) Cross-section view.

This will lower the nonuniformities in the electric field occurring due to the sharp electrode corners [58]. Furthermore a circular shaped aperture, concentric to the electrode stack, will produce constant thickness of the dielectric membrane around the floating gate electrode of the ISFET.

8.3.2 Sensor-system-on-chip integration

Integrating two or more sensor subsystems on a single chip that operate simultaneously, creates possibility of interference between them. Current work presents a sensor system that cannot operate simultaneously. This is based on the fact that each of the two sensor system requires a different potential level on the Ag/AgCl reference electrode. Since the reference electrode is common for the two sensor arrays, it can supply only one bias voltage level at a time. This issue can be resolved by integrating the Coulter counter electrode pair on the chip in a form of half-rings (Electrode 1 and Electrode 2) laid out around the sense micro-pore as depicted in Figure 8.5, hence removing the need for the off-chip electrode. Furthermore designing the electrode stack layout as entirely embedded into the intra-layer-dielectric (SiO_2) with a passivation layer (Si_3N_4) insulating it on the top will prevent metal oxidation. This will enable more stable long term impedance measurement since the

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metal electrode will not oxidise as it would while in a direct contact with an electrolyte solution.

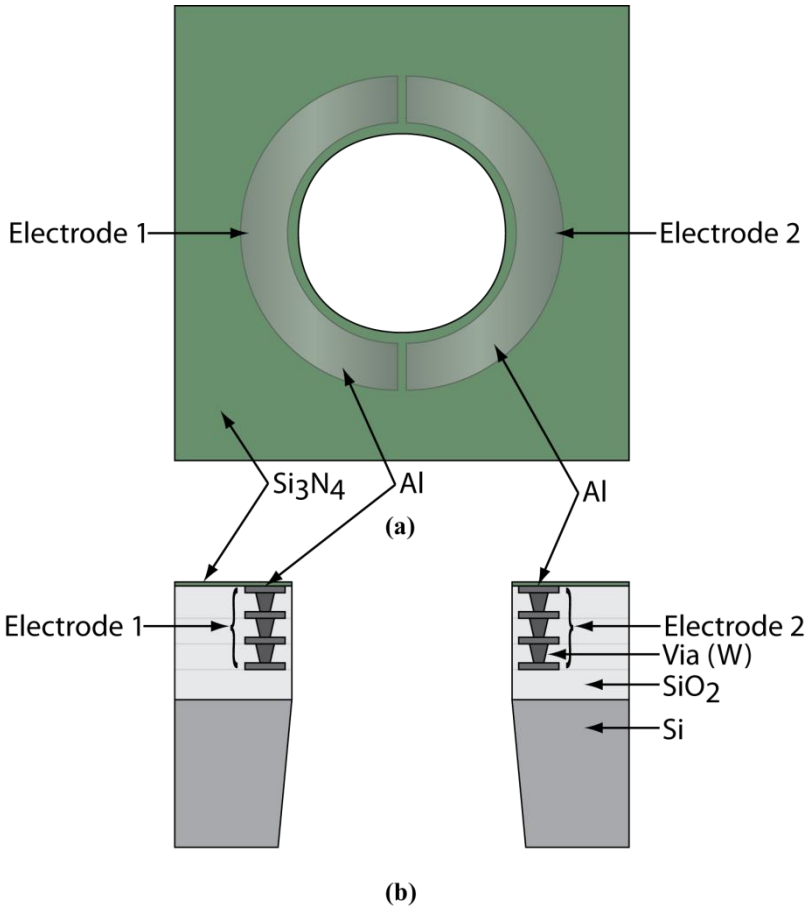

Figure 8.5: Half-rings electrode pair. (a) Top view, (b) Cross-section view.

To increase the sensing area of the electrode pair, multiple metal layers used in CMOS process can be stacked around the aperture and connected by process vias (Figure 8.5 (b)). This sensor structure in conjunction with a readout circuit operating at higher stimulus frequencies (outlined in Section 8.2.1) and improved on-chip membrane design (Section 8.2.2) will enable higher device throughput without increasing the number of the sense apertures. On the other hand this solution will allow only one sensor per aperture unless a CMOS process with a greater number of metal layers is used. Since the reference electrode is not required for this Coulter counter subsystem the flow-through ISFET array can be put into simultaneous operation with it by providing bias voltage through the Ag/AgCl electrode at the desired DC level required for the ion sensor operation.

The CMOS-MEMS device based on a standard semiconductor foundry process developed during this research work is not limited to the two sensors types. Other kinds of sensor structures utilising various sensing mechanisms (see Section 2) can be embedded

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into the MEMS platform. This will develop a highly integrated sensing system recording even more analyte specific parameters.

8.4 Summary

During this research work a sensor-system-on-chip has been successfully developed. Starting on an initial concept through the post-processing and encapsulation phases and finishing on a final test bench experiments in which the device was put into operation for biological cell sensing. Both sensor subsystems working in a flow-through mode of operation were able to detect cells suspended in an aqueous solution. Various implementations of the Coulter counter have been achieved in prior art [7]. However the level of miniaturisation and sensor system integration achieved in this work has significantly advanced the field by producing a scalable flow-through sensor array with integrated electronics manufactured in a 0.35 μm standard CMOS process. The work has demonstrated that the resultant system could record analyte properties by using an AC Coulter counter. Furthermore, a flow-through ISFET array has been utilised to detect the biological cells according to the charge carried on their membrane which is a novel usage of a well established CMOS based pH meter. Consequently, this CMOS-MEMS device now has the potential to develop into a micro-total-analysis-system that could provide deeper insight into the cell morphology by recording their physical and chemical properties. Indeed, the result of this research could lead to a novel highly miniaturise and portable cell-based screening tool that delivers multi-parametric data in real-time to the healthcare personnel.

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A Symbol Definitions

Table A.1 contains a description of the symbols used throughout this thesis.

Symbol	Description	Units	Value
A	(a) Area (b) Gain	m^2 V/V	
C	Capacitance	F	
D	Aperture diameter	m	
d	Particle diameter	m	
E	Electrode potential	V	
ε_0	Vacuum permittivity	F/m	8.85×10^{-12}
ε_r	Relative permittivity	F/m	
F	Faraday constant	C/mol	96.48×10^{3}
f	Frequency	Hz	
$\tilde{f}_{CM}$	Clausius-Mossotti factor	/	
G	Geometric constant	/	
γ_B	Body effect coefficient	$V^{1/2}$	
I	Current	A	
J	Current density	A/m^2	
K	Dissociation constant	/	
k	Boltzmann constant	J/K	1.38×10^{-23}
$\vec{k}_p$, $\overleftarrow{k}_p$	Heterogeneous rate constants for the forward and reverse ionic fluxes	/	
k'	Process transconductance parameter	A/V^2	
L	Length	m	
λ	Chanel length modulation parameter	V^{-1}	
μ	Mobility	$m^2/V\ s$	
η	Overpotential	V	
N_X	Density of active groups X	m^2	
pH	Hydrogen ion concentration	pH	
π	Pi-number	/	3.1415
φ	Volume fraction	/	
ϕ	Interface potential	V	
$\Delta\phi$	Potential difference across the interface	V	
Φ	Work function	eV	
Q	Charge density	C/m^2	
q	Electric charge	C	
R	(a) Molar gas constant (b) Resistance	J/mol K Ω	8.31
ΔR	Resistance change	Ω	
r	Radius	m	
σ	Conductivity	S/m	
σ_0	Surface charge density	$C/\ m^2$	
T	Absolute temperature	K	298

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Continued from prior page			
τ	Characteristic relaxation time constant	s	
V	Voltage	V	
ΔV	Voltage change	V	
W	Width	m	
ω	Angular frequency	rad/s	
ρ_m	Electrolyte resistivity	Ω m	
$[Xp]$	Ion concentration of species X	Mol	
χ	(a) Normalised net charge	m^2	
	(b) Surface dipole potential	V	
Z	Impedance	Ω	
z	Formal ionic charge	/	
ζ	Zeta potential	V	

Table A.1: Symbol definitions.

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B Nomenclature

Table B.1 contains a definition of the acronyms used throughout this thesis.

Acronym	Description
AC	Alternating Current
AMS	Austriamicrosystems
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BEOL	Back End Of the Line
BPSG	Boron-Phosphorus doped Silicate Glass
BSIM	Berkeley Short-Channel IGFET Model
CIP	Cleaning In Place
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapour Deposition
DAQ	Data Acquisition
DARPA	Defence Advanced Research Project
DC	Direct Current
DeMux	Demultiplexer
DI water	Deionised water
DNA	Deoxyribonucleic Acid
DNQ	diazonaphtoquinone
DRC	Design Rule Check
DRIE	Deep Reactive Ion Etching
DSP	Digital Signal Processing
dsDNA	Double stranded DNA
DUT	Device Under Test
DVD-ROM	Digital Versatile Disc Read Only Memory
EDA	Electronic Design Automation
EDL	Electrical Double Layer
EIS	Electrolyte Insulator Semiconductor
ERC	Electrical Rule Check
ESD	Electrostatic Discharge
FEOL	Front End Of the Line
FET	Field Effect Transistor
FIB	Focussed Ion Beam
FR	Flame Resistant
GDSII	Gerber Data Stream Information Interchange
GPIB	General Purpose Interface Bus
GUI	Graphical User Interface
I-AMP	Instrumentation Amplifier
ICP	Inductively Coupled Plasma
IDE	Integrated Development Environment
IEP	Isoelectric Point

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Continued from prior page

IGFET	Isolated Gate FET
IHP	Inner Helmholtz Plane
IMD	Intra Metal Dielectric
I/O	Input/Output
ISE	Ion Selective Electrode
ISFET	Ion Sensitive FET
I-SINK	Current Sink
I-SOURCE	Current Source
LMIS	Liquid-Metal Ion Source
LOAC	Lab On A Chip
LPCVD	Low Pressure Chemical Vapour Deposition
LVS	Layout Versus Schematic
MCU	Microcontroller Unit
MEMS	Micro Electro Mechanical Systems
MIM	Metal Insulator Metal
MOSFET	Metal Oxide Semiconductor FET
MPW	Multi-Project Wafer
Mux	Multiplexer
µTAS	Micro Total Analysis Systems
n-MOSFET	n-type MOSFET
NSG	Non-doped Silicate Glass
OCP	Open Circuit Potential
OHP	Outer Helmholtz Plane
OP-AMP	Operational Amplifier
OS	Operating System
PCB	Printed Circuit Board
PDK	Process Design Kit
PDMS	Polydimethylsiloxane
PECVD	Plasma Enchance Chemical Vapour Deposition
PEEP	Polyetheretherketone
pH	Pondus Hydrogenii
PIP	Poly Insulator Poly
PMD	Pre Metal Dielectric
p-MOSFET	p-type MOSFET
poly	Polycrystalline silicon
PVC	Polyvinyl Chloride
PZC	Point of Zero Charge
QCM	Quartz Crystal Microbalance
qRE	Quasi Reference Electrode
RAM	Random Access Memory
RBC	Red Blood Cell
REFET	Reference FET
RF	Radio Frequency
RIE	Reactive Ion Etch
RNA	Ribonucleic Acid

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Continued from prior page	
SCE	Saturated Calomel Electrode
SDL	Schematic Driven Layout
SEM	Scanning Electron Microscope
SMU	Source Measure Unit
SoC	System on Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
ssDNA	Single stranded DNA
SSoC	Sensor System on Chip
STI	Shallow Trench Isolation
TG	Transmission Gate
USB	Universal Serial Bus
UV light	Ultraviolet light
VISA	Virtual Instrument Software Architecture
VLSI	Very Large Scale Integrated Circuits
WL-CSP	Wafer Level Chip Scale Packaging
XTAL	Crystal

Table B.1: Acronyms descriptions.

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C Precision Impedance Analyzer Calibration Procedure

Calibration procedure (Table C.1) of the Agilent 4294A was based on the operation manual [180, Section 6]. The procedure was executed for a four-terminal pair with 1 m extension cables. Note that the calibration procedure needed to be repeated after each change of the stimulus frequency.

Step	Description
I	1. Press the SOURCE key to set the stimulus voltage level. 2. In the same menu set the oscillator frequency and unit. 3. Set the stimulus frequency range by pressing the START and STOP hardkeys. 4. Choose stimulus sweep parameter located under SWEEP menu. 5. In the same menu set the number of data points per single sweep.
II	1. Mount in place and connect the extension adapter to the instrument.
III	1. Enable calibration menu by pressing CAL button on the front panel. 2. Navigate to an Adapter submenu and chose the appropriate adapter, confirm with ENTER.
IV	1. Go to Fixture compensation submenu. 2. Perform calibration with Open circuit (test fixture unconnected). 3. Perform calibration with Short circuit (test fixture shorted using appropriate BNC-BNC connector).
V	1. Chose the display scale by going to menu located under the SCALE REF hardkey. 2. Set the display format by going to FORMAT menu.
VI	1. Chose the measured values located under MEAS key.
VII	1. Connect the device under test and perform measurements.

Table C.1: Calibration procedure for the impedance analyzer.

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D Sensor System on Chip Circuit Schematics

The circuit schematics for the sensor-system-on-chip are shown in Figures D.1 to D.13.

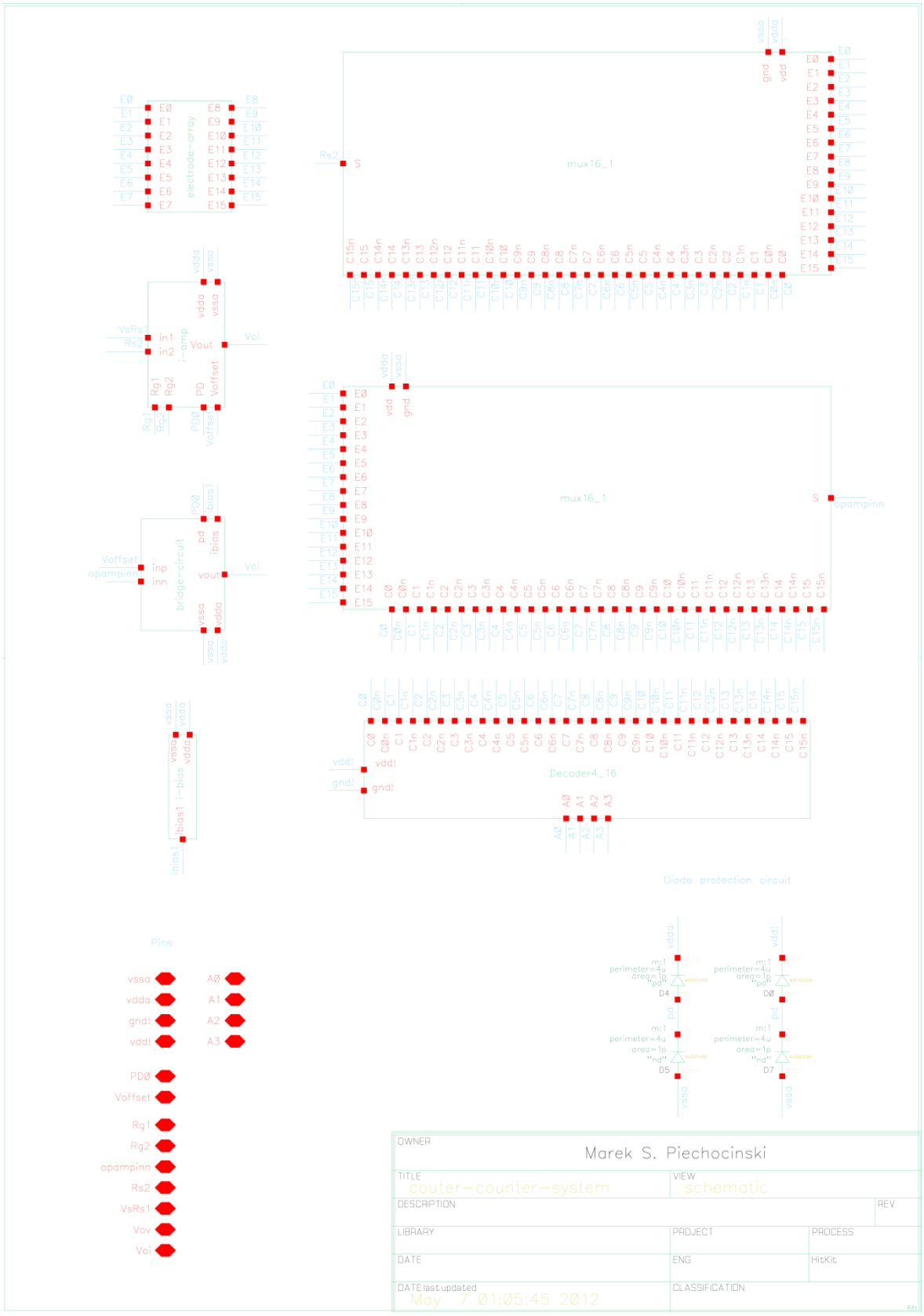

Figure D.1: Circuit schematic of the cell “coulter-counter-system”.

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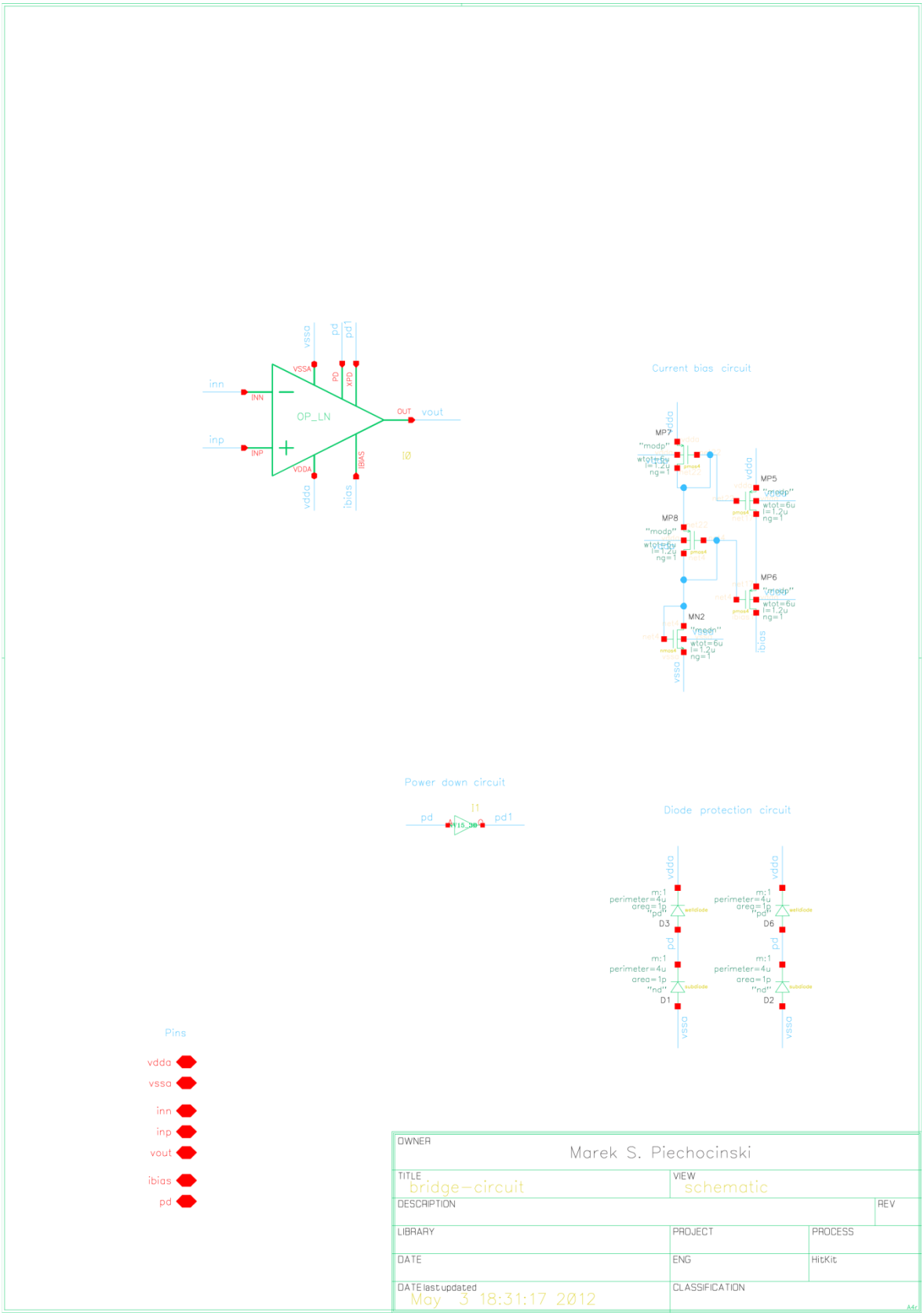

Figure D.2: Circuit schematic of the cell "bridge-circuit".

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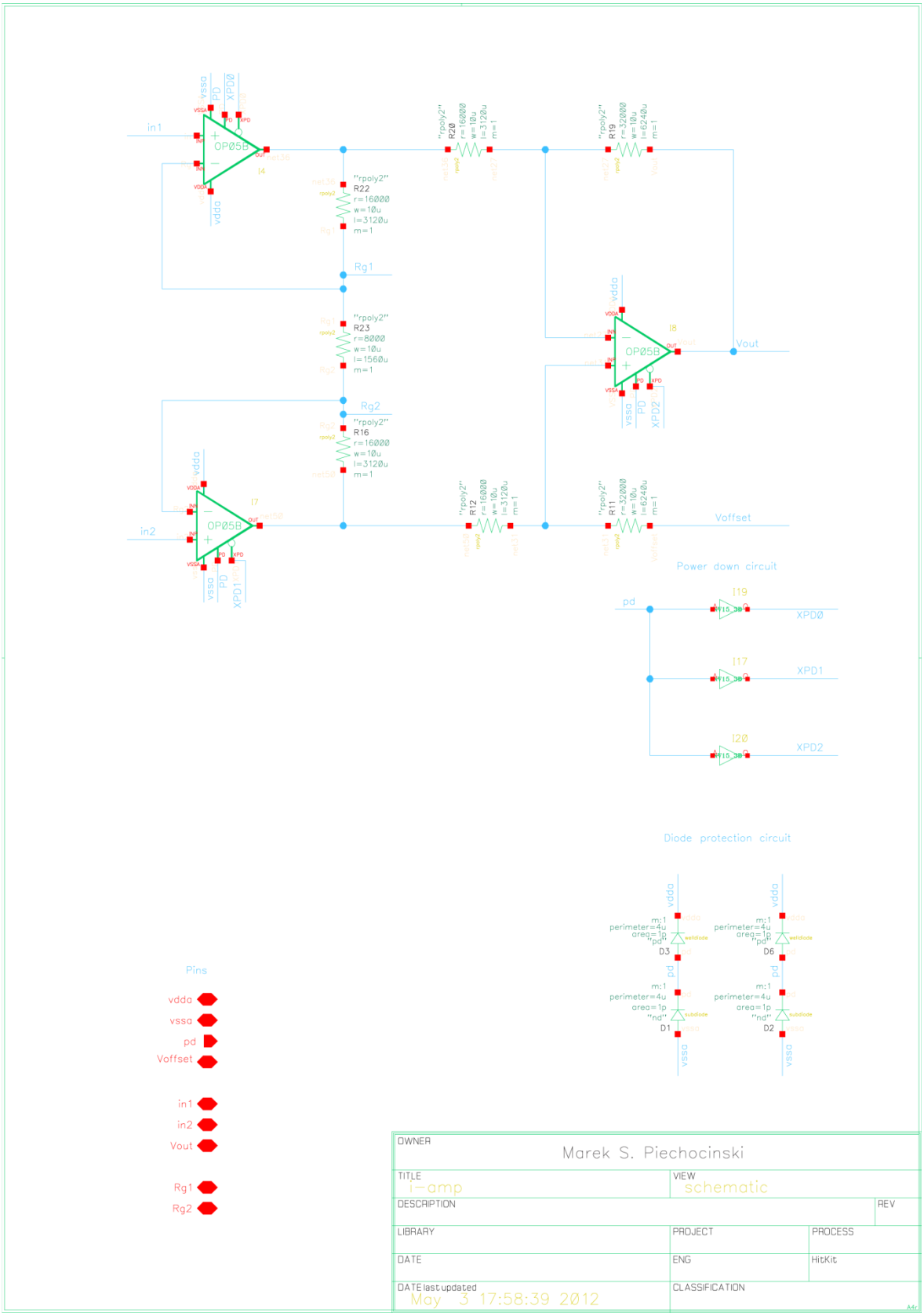

Figure D.3: Circuit schematic of the cell "i-amp".

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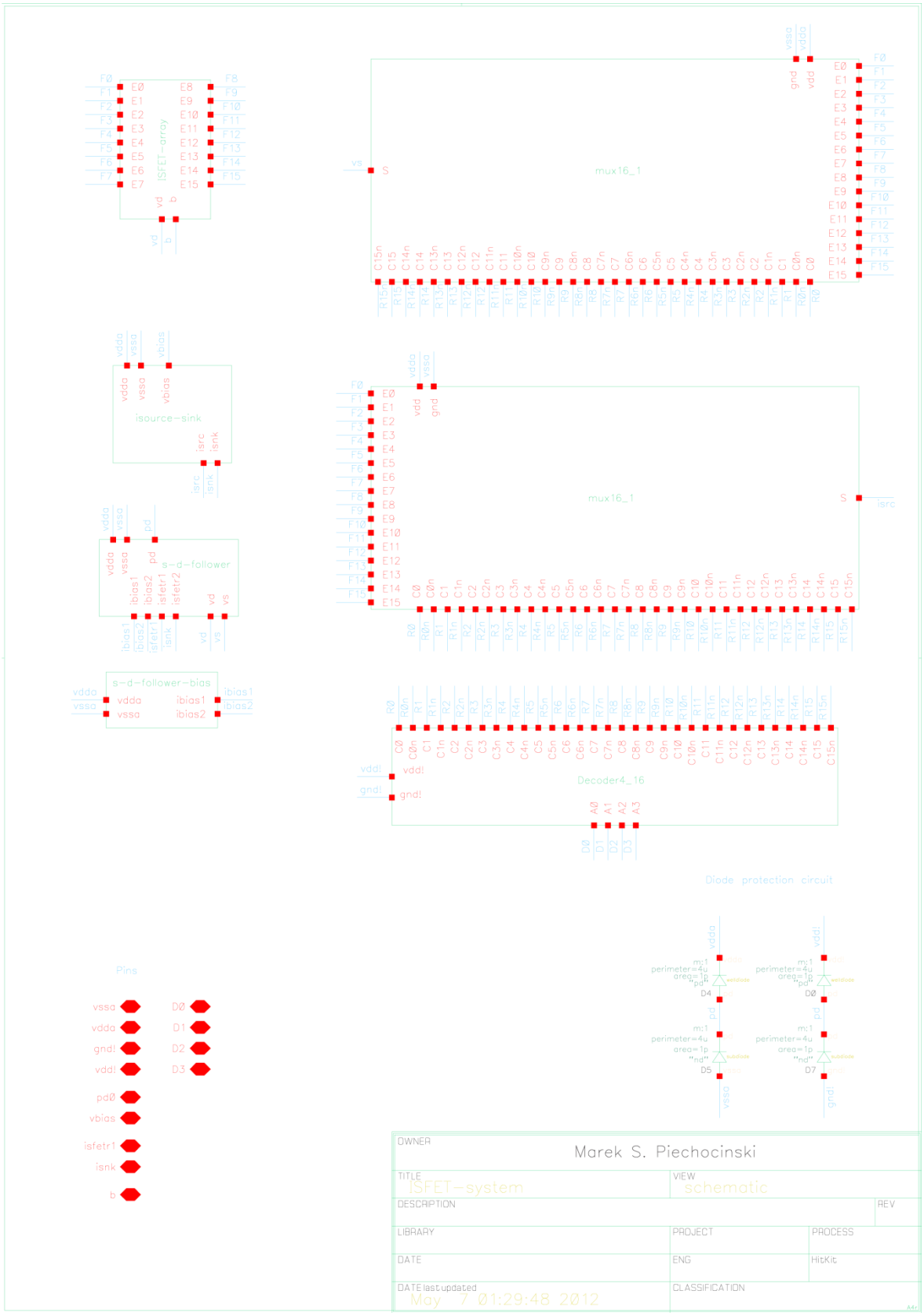

Figure D.4: Circuit schematic of the cell “isfet-system”.

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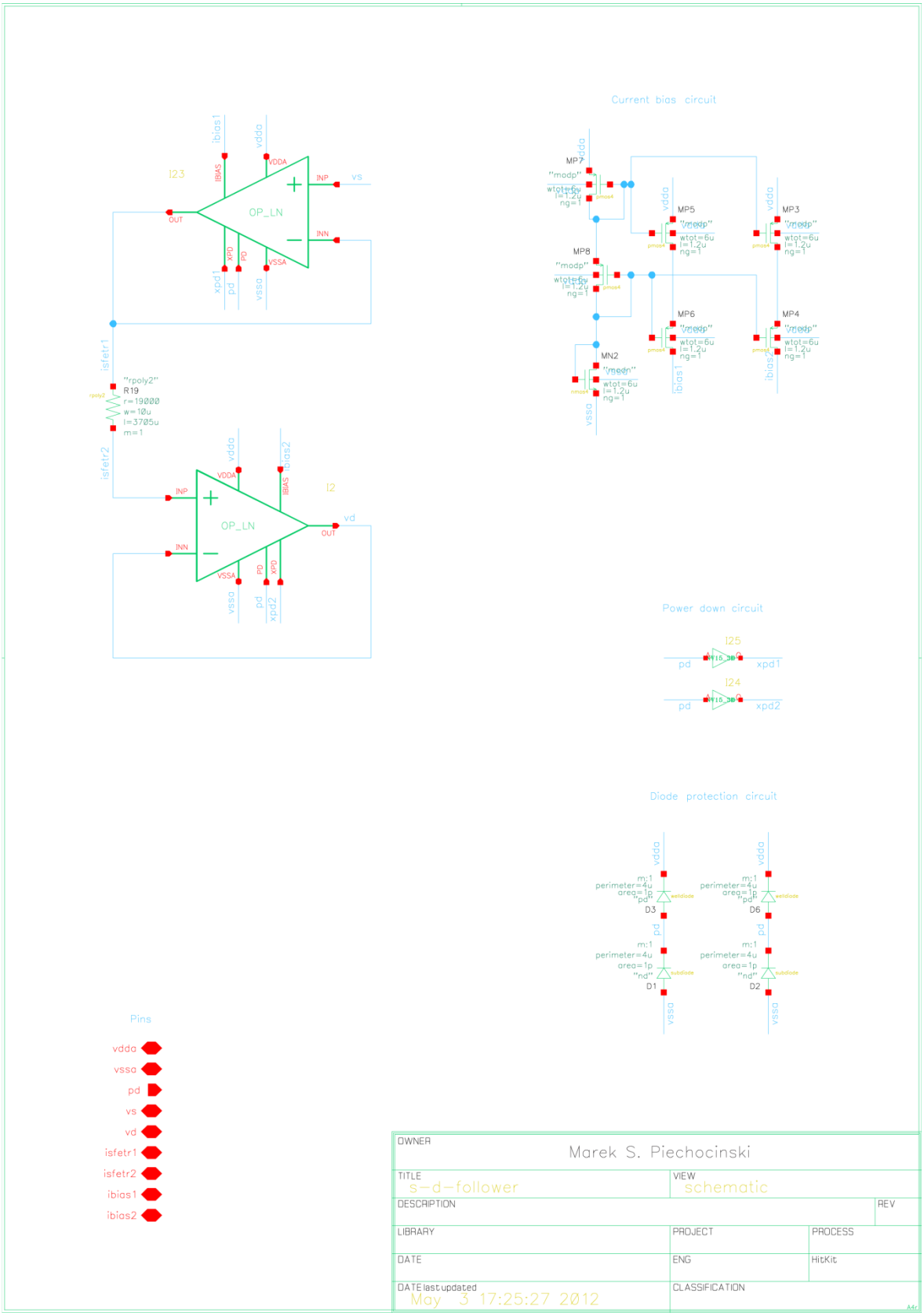

Figure D.5: Circuit schematic of the cell "s-d-follower".

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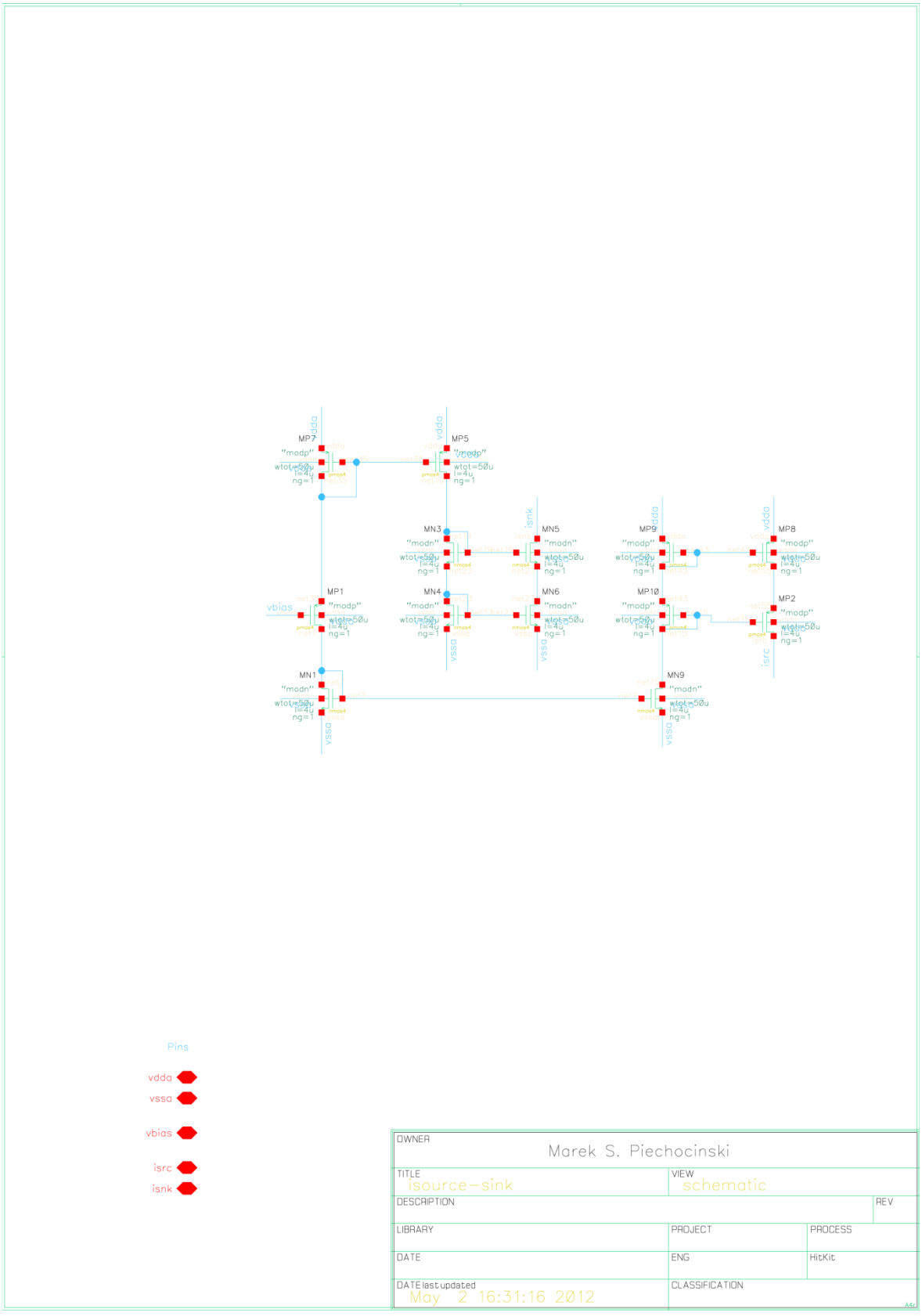

Figure D.6: Circuit schematic of the cell "isource-sink".

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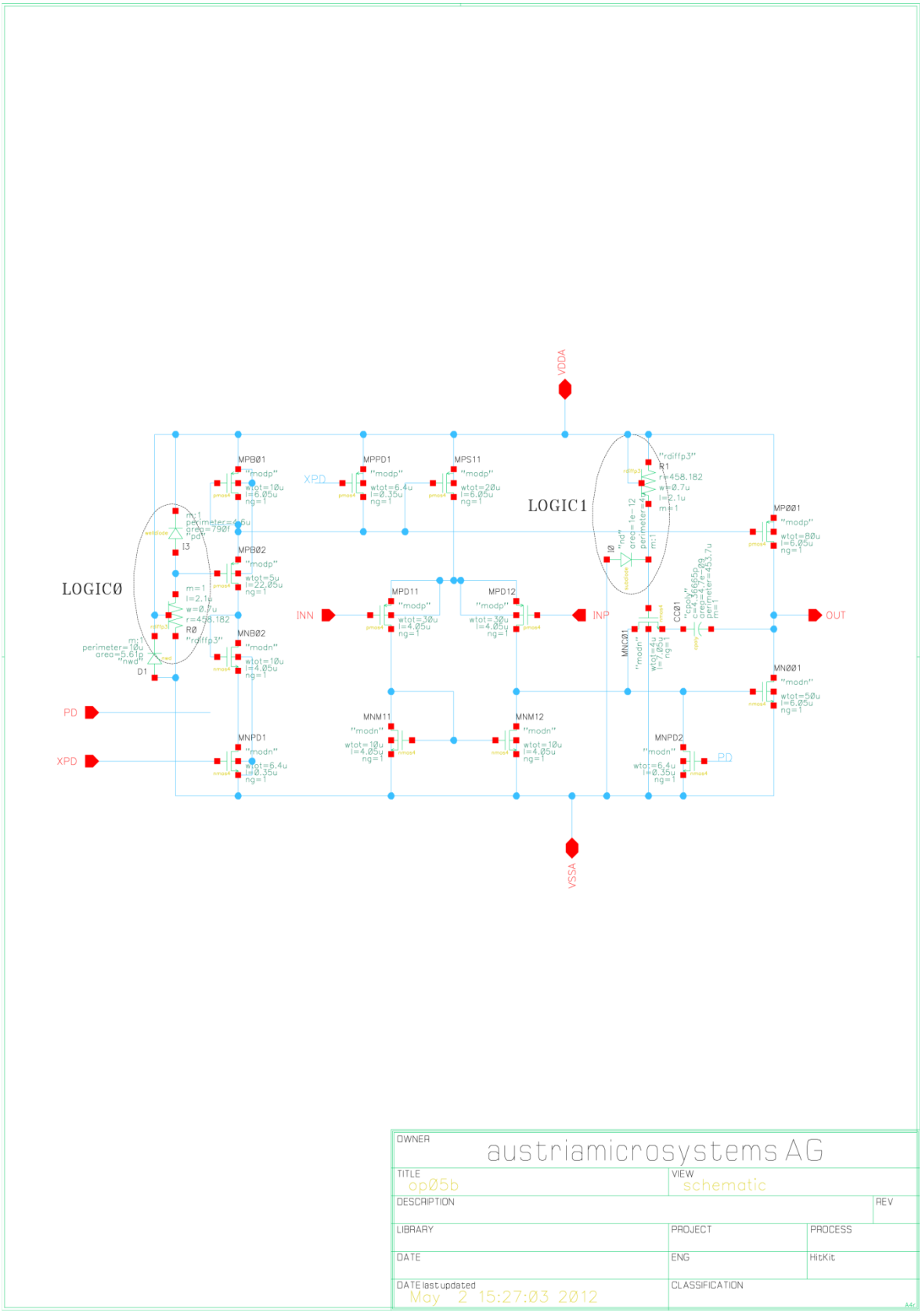

Figure D.7: Circuit schematic of the cell “op05b”.

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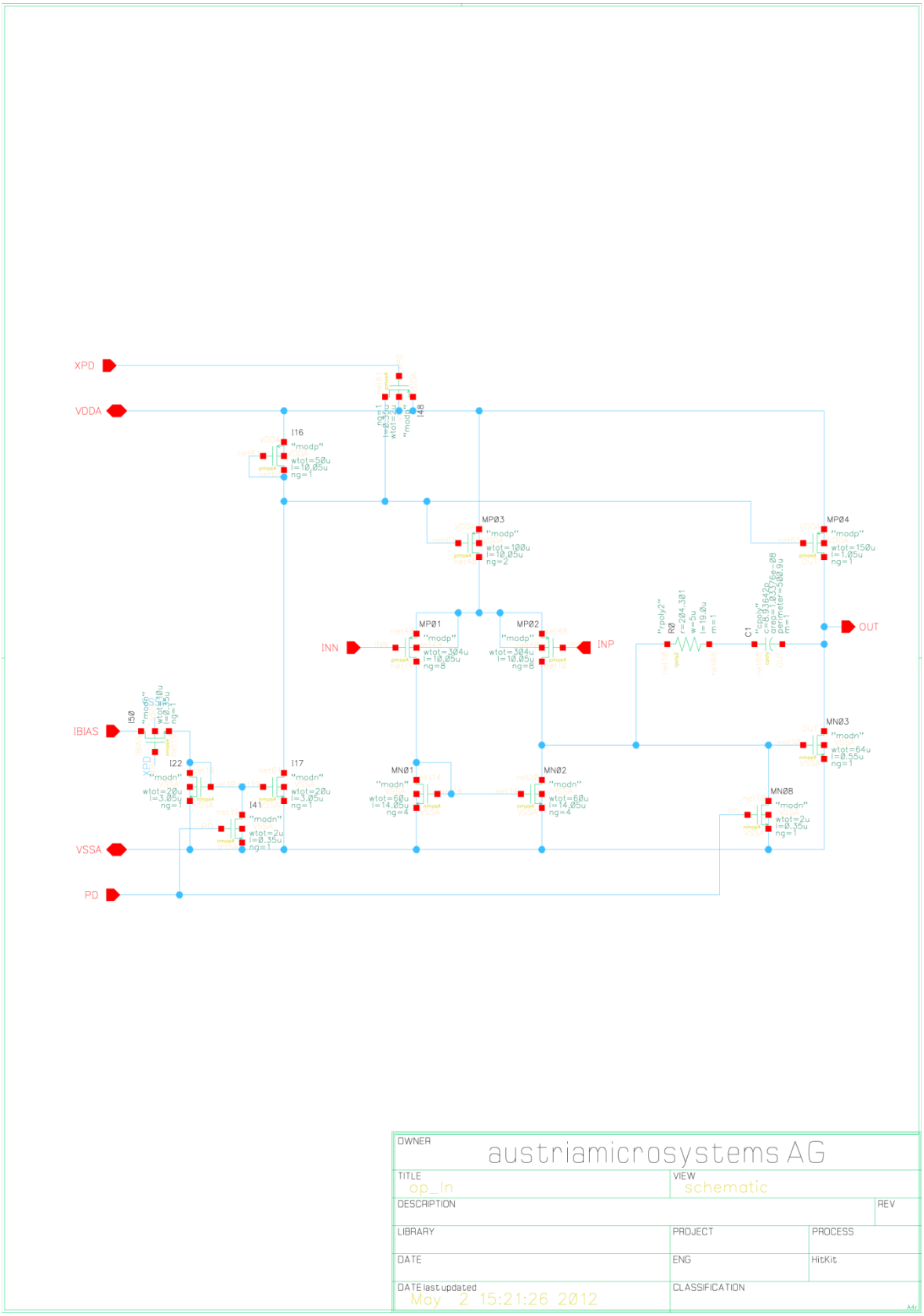

Figure D.8: Circuit schematic of the cell “op_ln”.

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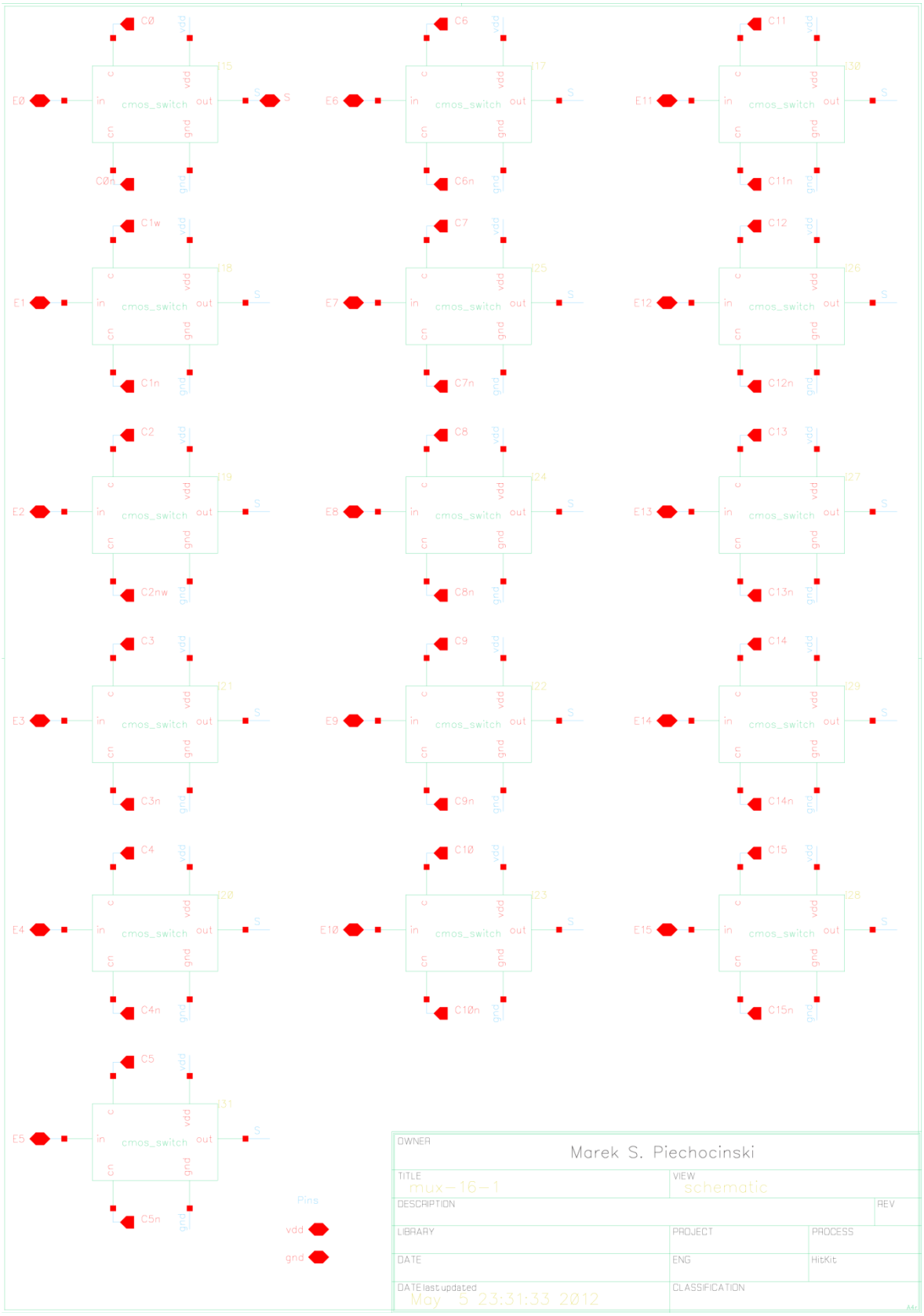

Figure D.9: Circuit schematic of the cell "mux-16-1".

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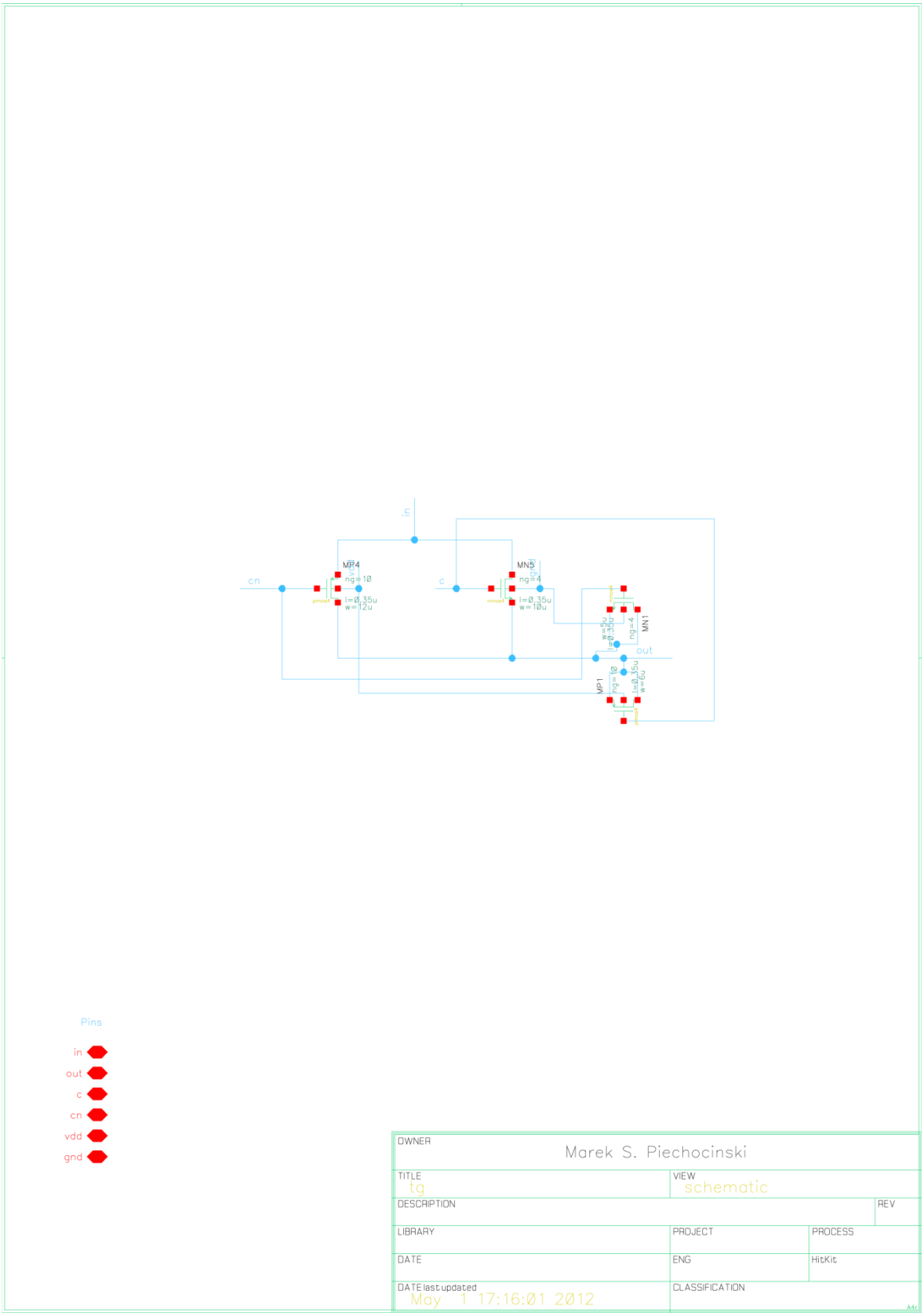

Figure D.10: Circuit schematic of the cell “tg”.

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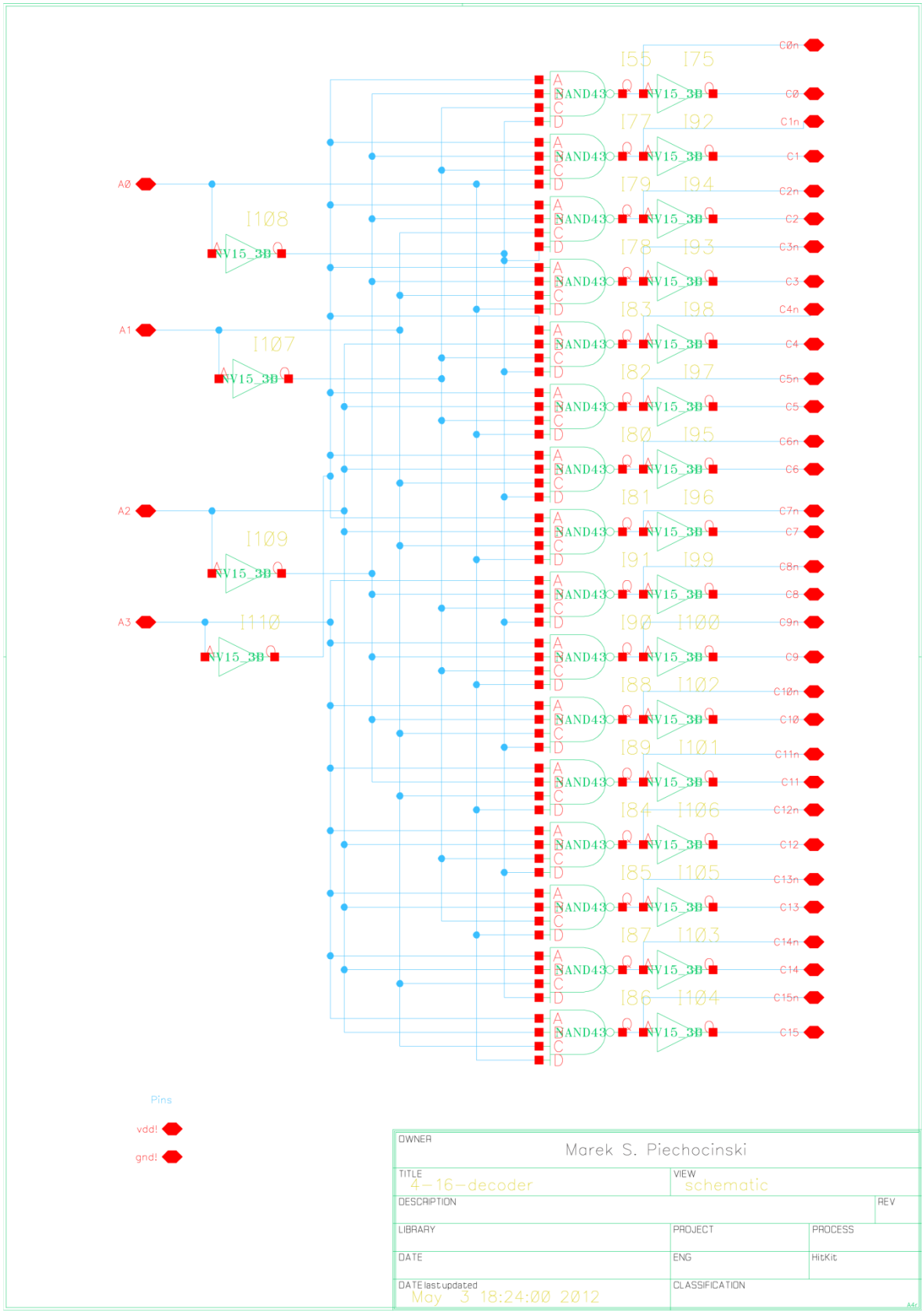

Figure D.11: Circuit schematic of the cell "4-16-decoder".

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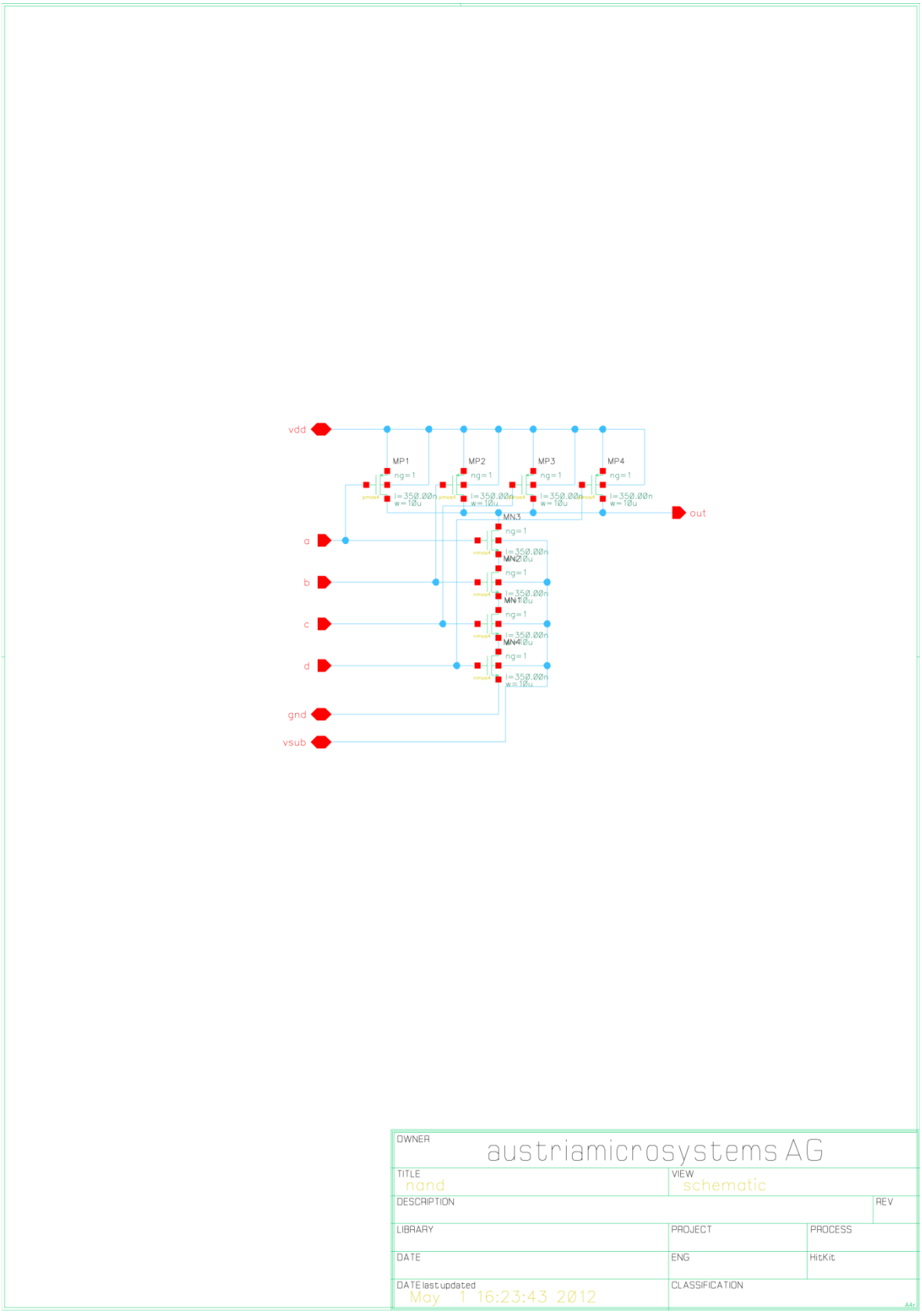

Figure D.12: Circuit schematic of the cell “nand”.

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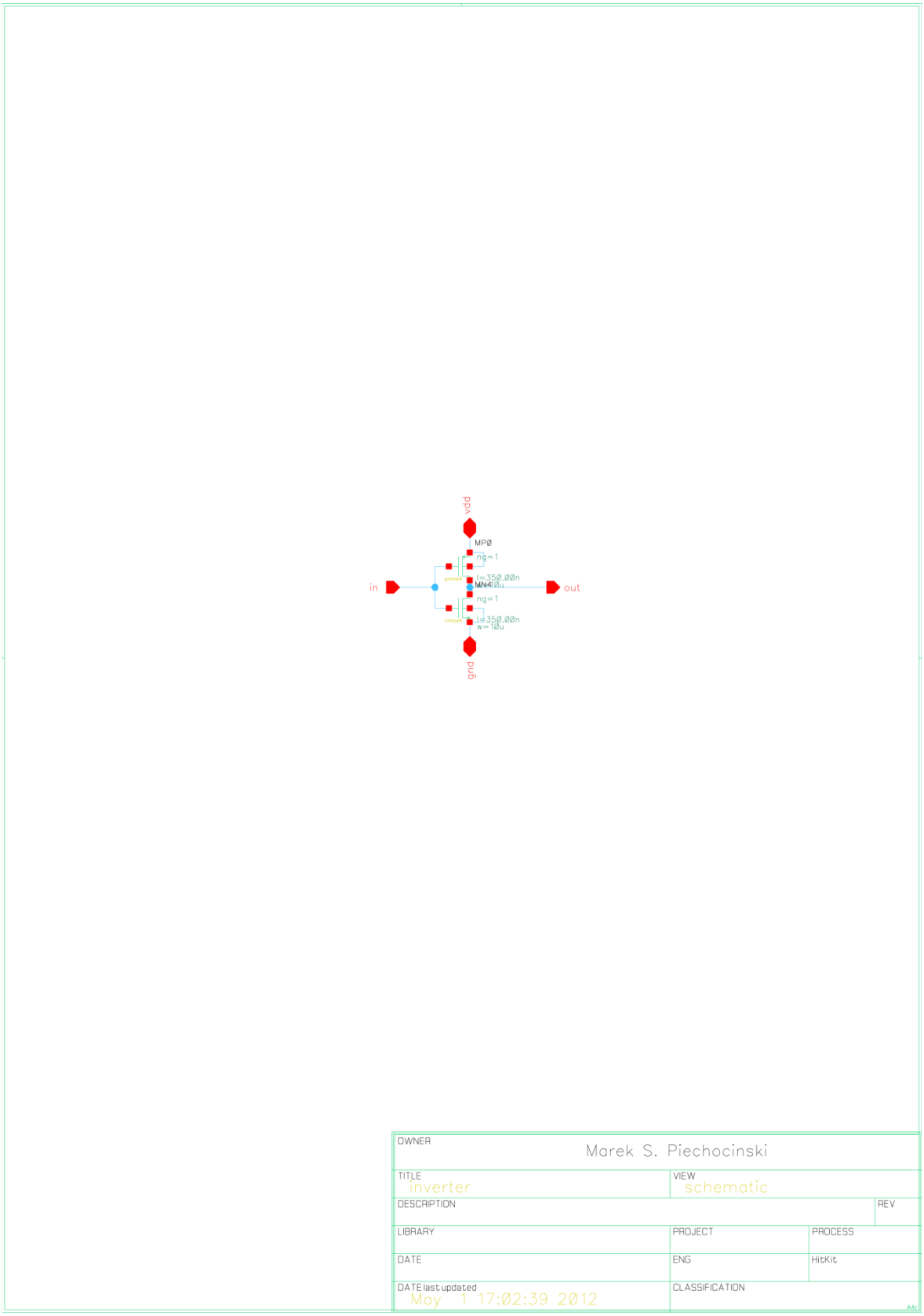

Figure D.13: Circuit schematic of the cell “inverter”.

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E Source Code

The main modules of the DAQ and control software are shown in Figures E.1 to E.5.

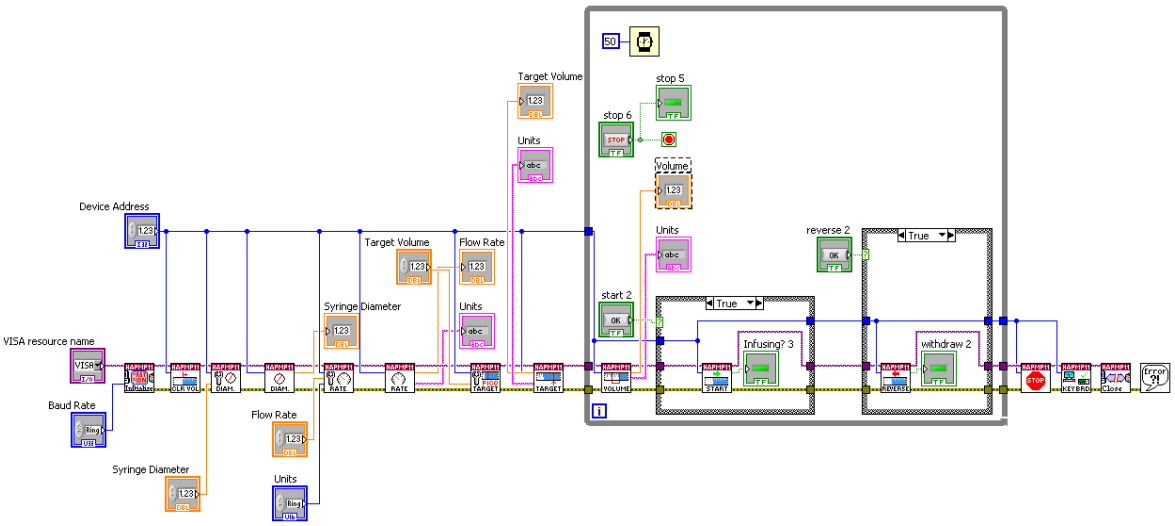

Figure E.1: Syringe pump control module.

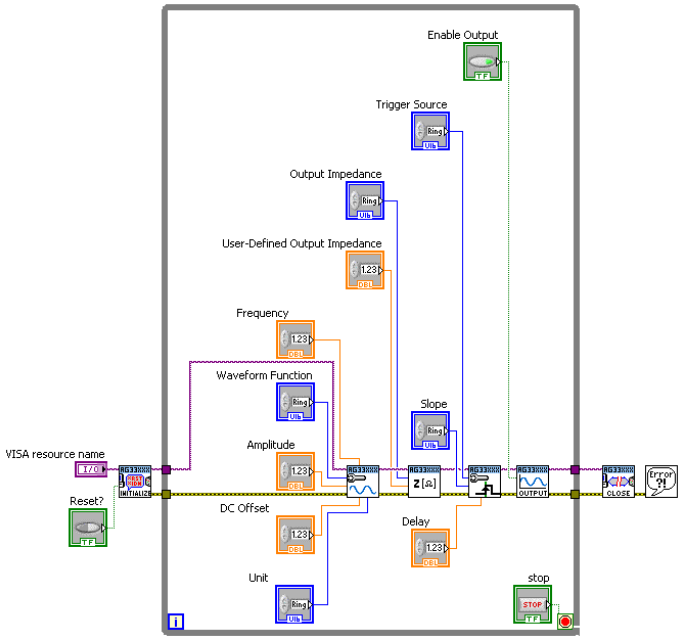

Figure E.2: Signal generator control module.

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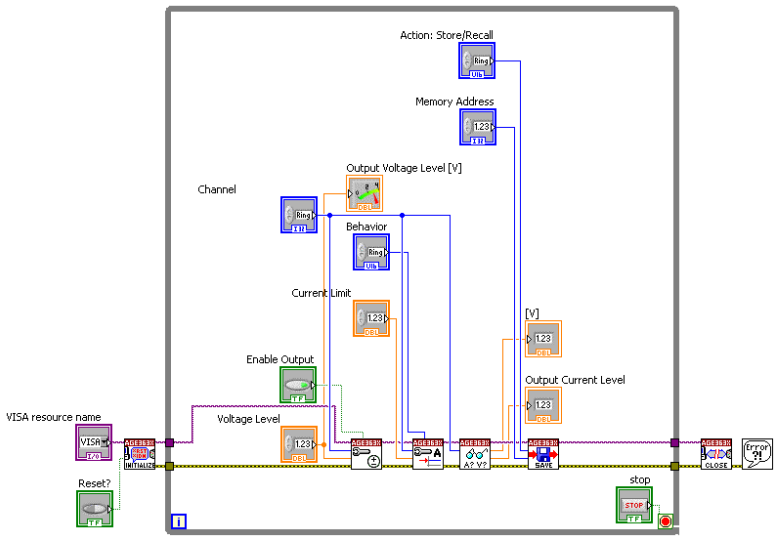

Figure E.3: DC power supply control module.

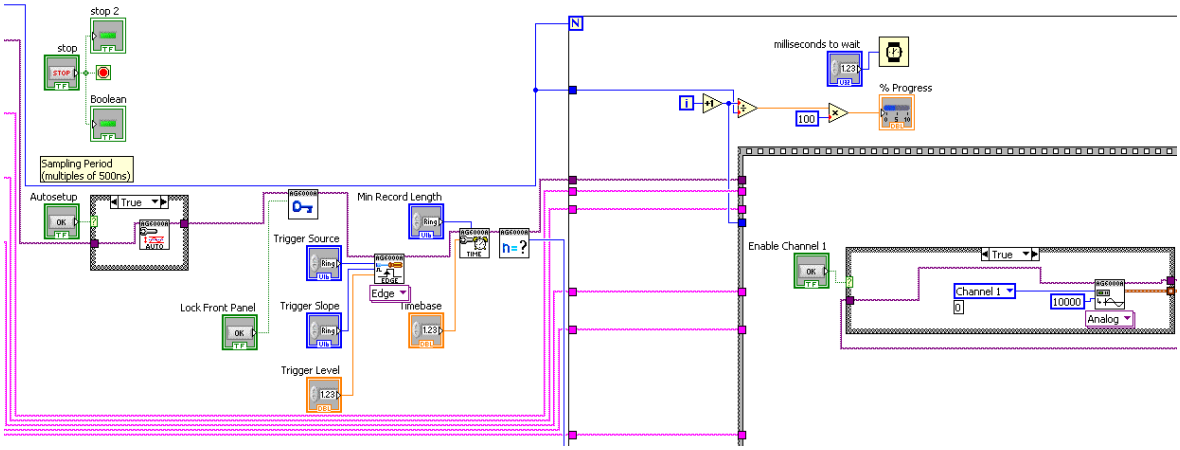

Figure E.4: Oscilloscope control module, channel 1 setup.

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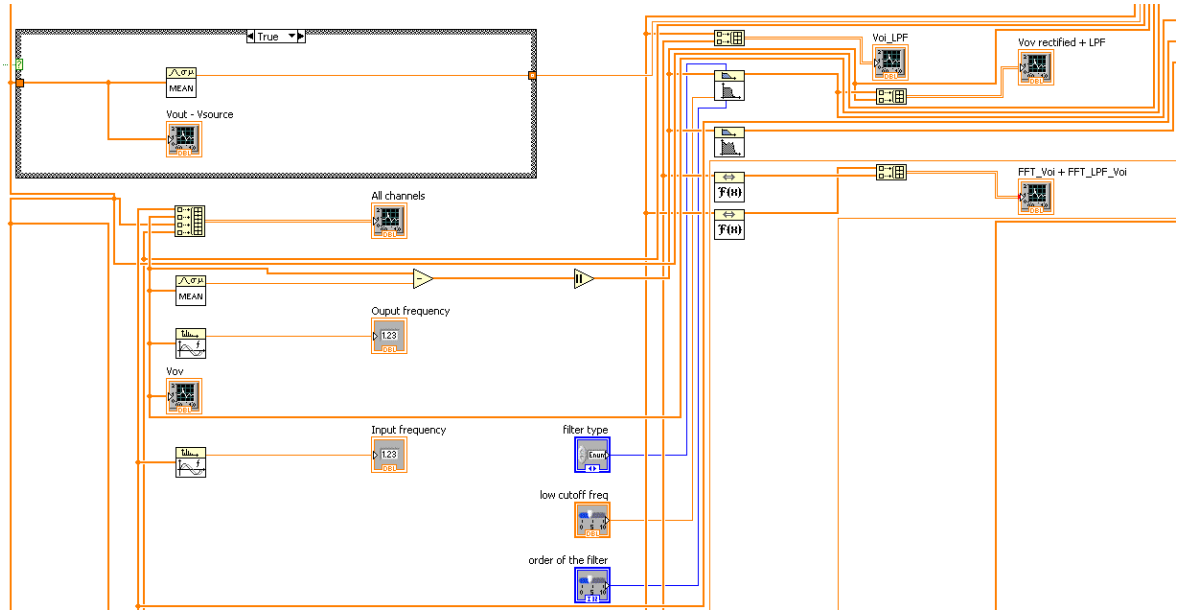

Figure E.5: DSP control module.

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